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Fieldbus Communications Controller

FB2050

DataSheet

Features

- Conforms to IEC 1158-2 / ISA SP50.02 Physical Layer Standard for Foundation Fieldbus
- Provides software selectable full and half duplex communications
- Automatic polarity detection and correction for incoming Manchester signal
- Software controlled FCS generation for transmitter and automatic frame check sequence (FCS) detection for receiver
- Compatible with most microprocessors and micro controllers with special Interface pins provided for the Motorola M68HC11 microprocessor
- RAM and PROM paging and chip-select logic provided to reduce system chip count
- 31.25 Kbits/sec data rate
- FCDS generation and detection
- Software controlled chip-select pins for I/O interface
- Memory management capabilities and additional interface logic for use with the M68HC11 and other microcontrollers

Pin Descriptions

The pins on the FB2050 can be divided into five functional groups:

- microprocessor interface
- chip-select
- memory paging
- receiver
- transmitter

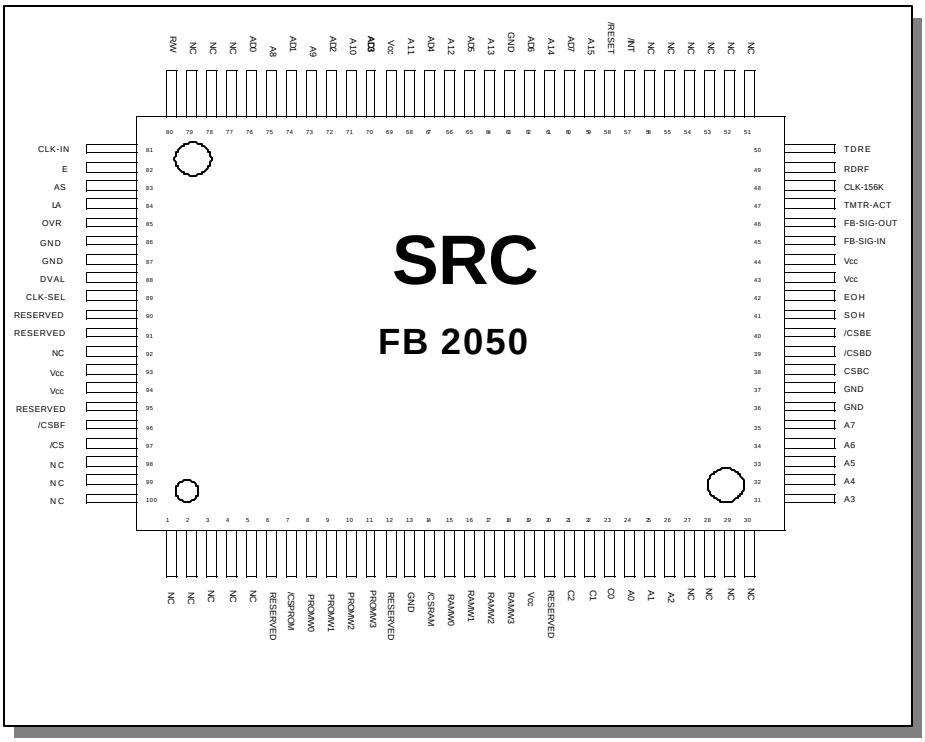


Figure 1 - Pin Designations

MICROPROCESSOR INTERFACE PINS

CLK-IN: Master Clock Input. All internal timing signals are derived from this clock. For low speed Fieldbus applications the frequency of this clock must be either 625 KHz ±0.2% or 1.25 MHz ±0.2%.

CLK-SEL: Input Clock Select; selects the CLK-IN frequency input.

High: 1.25 MHz **CLK-IN**
Low: 625 KHz **CLK-IN**

E: Input . Should be connected to the E clock of the M68HC11 controller. All read and write operations are synchronized with the positive cycle of this clock.

AS: This input should be connected to the AS output of the M68HC11. An active high pulse on this pin latches the low address bus, AD [7-0], into the internal 8-bit latch. The outputs of this latch is connected to pins A[7-0].

/CS: This pin should be connected to an active low pulse source synchronized with the other interface pins to provide pulses needed for read and write operations.

/R/W: This pin indicates the direction of data transfer between the FB2050 and the processor. A high signal indicates reading the FB2050. A low signal indicates writing to the FB2050.

/RESET: Hardware Reset. A low pulse on this pin resets the entire chip.

C[2-0]: Control Bus. These three lines are used to control all read and write operations of the FB2050 internal registers.

AD[7-0]: Multiplexed address/data bus.

A[15-8]: High bits of address bus.

A[7-0]: Outputs of the internal address latch. The low address is latched with an active high pulse on **AS.** This internal latch eliminates the necessity for an external address latch.

/INT: Interrupt request. This signal goes low when an unmasked internal interrupt source generates an interrupt request. The source of the interrupt can be identified by reading the interrupt status register.

C2	C1	C0	R/W	Operation *(synchronized with E)*
0	0	0	0	TRANSMITTER_BUFFER
0	0	1	0	TRANSMITTER_RESET
0	1	0	0	START_TRANSMISSION
0	1	1	0	RECEIVER_RESET
1	0	0	0	INTERRUPT_MASK
1	0	1	0	CONTROL_REGISTER_1
1	1	0	0	PROM_PAGE_REGISTER
1	1	1	0	RAM_PAGE_REGISTER
X	0	0	1	RECEIVER_BUFFER
X	0	1	1	STATUS_REGISTER_1
X	1	0	1	INTERRUPT_STATUS
X	1	1	1	STATUS_REGISTER_2

Table 1: Control Registers

CHIP SELECT PINS

/CSPROM: Provides an active low chip select pulse for the system PROM when the processor accesses address C000-FFFF or address 4000-7FFF.

/CSRAM: Provides an active low chip select pulse for the system RAM when the processor accesses address 0200-3FFF or address 8000-AFFF.

CBS: Creates an active high pulse when the processor accesses address BC00-BCFF.

/CSBD: Creates an active low pulse when the processor accesses address BD00-BDFF.

/CSBE: Creates an active low pulse when the processor accesses address BE00-BEFF.

/CSBF: Creates an active low pulse when the processor accesses address BF00-BFFF.

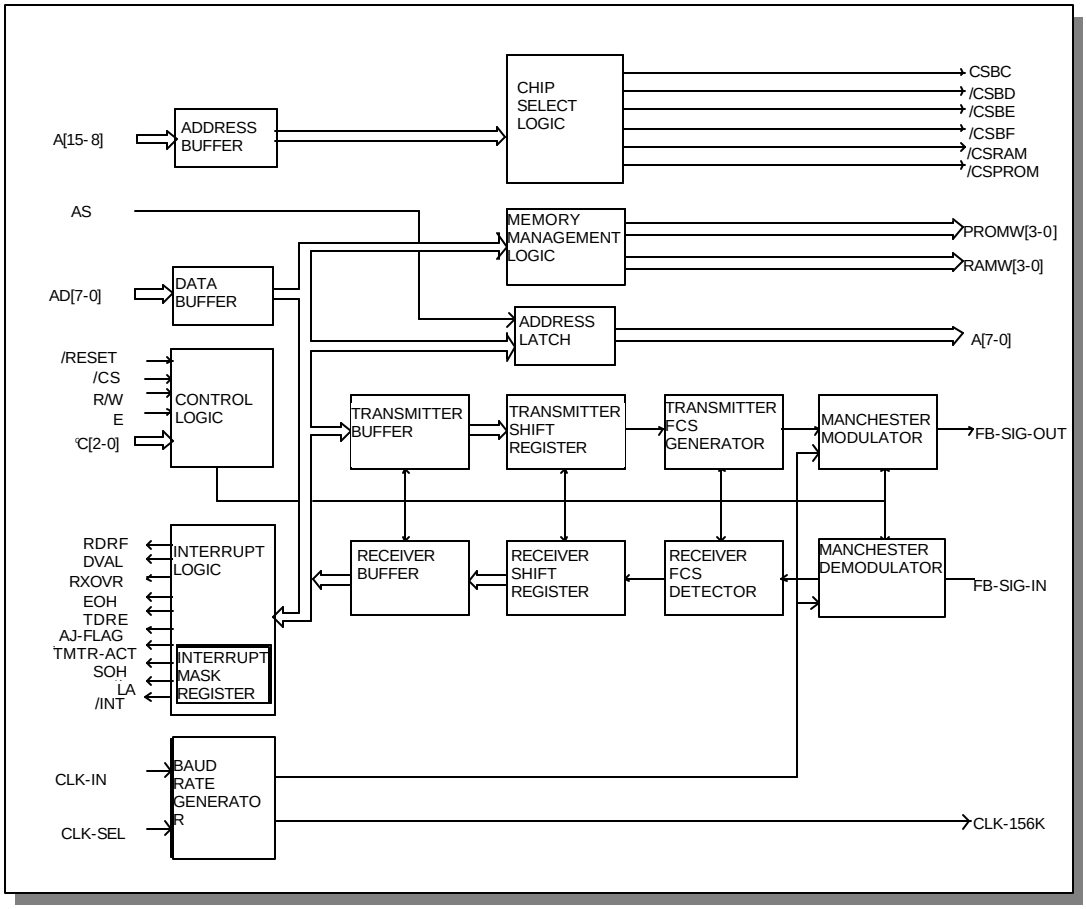


Figure 2 - Block Diagram

Pin Number	Name	Type	Description
7	/CSPROM	Output	Chip select for external PROM
8-11	PROMW(0-3)	Output	PROM Page selector bus
14	/CSRAM	Output	Chip select for external RAM
15-18	RAMW10(0-3)	Output	RAM page selector bus
21-23	C(2-0)	Input	Control Bus
24-26	A(0-2)	Output	Address latch output
31-35	A(3-7)	Output	Address latch output
38	CSBD	Output	Active high chip select @ BCXX
39	/CSBD	Output	Active low chip select @ BDXX
40	/CSBE	Output	Active low chip select @ BEXX
41	SOH	Output	Start of header delimiter indicator
42	EOH	Output	End of header delimiter indicator
45	FB-SIG-IN	Input	Fieldbus signal input pin
46	FB-SIG-OUT	Output	Fieldbus signal output pin
47	TMTR-ACT	Output	Transmitter activity signal
48	CLK-156K	Output	Output clock: 156.25 Khz
49	RDRF	Output	Receiver data register full
50	TDRE	Output	Transmitter data register emoty
57	/INT	Output	Interrupt request signal
58	/RESET	Input	Master reset
59,61,64,66	A(15-12)	Input	Address bus
68,71,73,75	A(11-8)	Input	Address bus
60,62,65,67	AD(7-4)	Input/Output	Multiplexed address/data bus
70,72,74,76	AD(3-0)	Input/Output	Multiplexed address/data bus
80	R/W	Input	Read/write
81	CLK-IN	Input	Input clock (25 Khz or 62 Khz)
82	E	Input	E Clock from M68HC11
83	AS	Input	Address strobe from M68HC11
84	LA	Output	Receiver activity
85	RX-OVR	Output	Receiver overrun
89	CLK-SEL	Input	Clock select
6,12,20,90,91,95	RESERVED	-	-
96	/CSBF	Output	Active low chip select @ BFXX
97	/CS	Input	/CS signal
13,36,37,63,86,87	GND	-	Ground
19,43,44,69,93,94	Vcc	-	Supply voltage +/- 5V
1-5	Do Not Connect	-	-
27-30	Do Not Connect	-	-
51-56	Do Not Connect	-	-
77-79	Do Not Connect	-	-
92,98,99,100	Do Not Connect	-	-

Table 2 - Pin Outs

MEMORY PAGING PINS

PROMW[3-0]: Outputs of the register containing the page address for the PROM. Active during any access to memory page 4000-7FFF. When any other address is accessed, the output of these pins is zero.

RAMW[3-0]: Outputs of the register containing the page address for the RAM. Active during any access to memory page 0200-03FF. When any other address is accessed, the output of these pins is zero.

RECEIVER PINS

FB-SIG-IN: Fieldbus Digital Input Pin. CMOS level input. Proper filtering and level conversion is required for the Fieldbus line.

RDRF: Receiver data register full. This signal goes high when there is a valid byte in the receiver data register. It goes low when the processor reads the receiver data. This signal is one of the sources that causes the INT signal to go low and can also be used as an independent interrupt request line.

LA: Receiver line activity. This signal goes high when the controller detects any transitions on the receiver line and remains high until the the absence of activity on the line for app. 160 µs.

DVAL: This signal goes high after the start delimiter has successfully been received. It goes low if the controller receives a missing transition (N+ or N-). This signal is one of the sources that causes the INT signal to go low and can also be used as an independent interrupt request line.

RX-OVR: Receiver Overrun Flag. This signal goes high when the processor fails to read the receiver data register and a new byte is received. This signal is one of the sources that causes the INT signal to go low and can also be used as an independent interrupt request line.

SOH: Receiver Start of Header Delimiter. This signal goes high after successful detection of start delimiter and goes low when LA goes low.

EOH: Receiver End of Header Delimiter. This signal goes high after successful detection of end delimiter and goes low when LA goes low. This signal is one of the sources that causes the INT signal to go low and can also be used as an independent interrupt request line.

TRANSMITTER PINS

FB-SIG-OUT: Fieldbus Digital Output Pin. This is a CMOS output buffer during transmission and is tristate when the transmitter is idle.

TDRE: Transmitter Data Register Empty. This signal goes high when the transmitter buffer is empty. It goes low when the transmitter data register is written into. This signal is one of the sources that causes the INT signal to go low and can also be used as an independent interrupt request line.

TMTR-ACT: Transmitter Activity. This signal is low when the transmitter is idle. It goes high as soon as the transmitter starts its activity and stays high until the end of the message.

CLK-156K: 156.25KHz Clock Output for general purpose application.

REGISTER DEFINITIONS

Control bus input pins C[2-0] control all read and write operations for the FB2050. By connecting these pins to output pins A[2-0] these operations can be performed by accessing specific addresses of the memory map. For example, connecting the output pin /CSBF to the input pin /CS will connect the FB2050 to address page BFXX without the need for external chip select components. Any of the other active low chip select outputs can also be selected in

TRANSMITTER BUFFER

When the FB2050 transmitter is on, writing to address BF00 transfers the byte on the data bus, AD[7-0], into the transmitter data register. To avoid transmitter overrun and assure that the transmitter is ready to receive the next byte to be transmitted, the TDRE flag inside the STATUS_REGISTER_1 should be checked prior to a transmitter write operation.

TRANSMITTER_RESET

This reset operation has the same effect as a hardware reset on the transmitter.

The receiver chip select modules are not affected by this operation.

START_TRANSMISSION

A write to this address forces the FB2050 transmitter out of the idle state. The value of the data bus during this write is irrelevant. After the transmitter is turned on it immediately starts to transmit a 16-bit preamble followed by the SOH and by the byte stored in the transmission data register. In half duplex mode, the transmitter checks the status of the Field Bus Line before granting a start of transmission.

IMPORTANT: *The first byte of the message must be written immediately after a START_Transmission is issued.*

Register	Address BFXX + C(2-0)	Operation
TRANSMITTER_BUFFER	BF00	write only
TRANSMITTER_RESET	BF01	write only
START_TRANSMISSION	BF02	write only
RECEIVER_RESET	BF03	write only
INTERRUPT_MASK	BF04	write only
CONTROL_REGISTER_1	BF05	write only
PROM_PAGE_REGISTER	BF06	write only
RAM_PAGE_REGISTER	BF07	write only
RECEIVER_BUFFER	BF00	read only
STATUS_REGISTER_1	BF01	read only
INTERRUPT_STATUS	BF02	read only
STATUS_REGISTER_2	BF03	read only

RECEIVER_RESET

This reset operation has the same effect as hardware reset on the receiver.

The transmitter module and the chip select module are not affected by this operation.

INTERRUPT_MASK

This register is used to enable or disable the interrupt source generated by the FB2050. During RESET this register is cleared.

The receiver and chip select modules are not affected by this operation.

	7	6	5	4	3	2	1	0
	RDRF	DVAL	RX-FCS	EOH	RX-OVR	DLL-LOCK	TMTR-ACT	TDRE
RESET	0	0	0	0	0	0	0	0

TDRE: Interrupt on transmitter data register empty. Indicates that data may be written into the transmitter data register.

0 = Disable
1 = Enable

TMTR-ACT: Interrupt on end of transmission. Indicates that entire transmission frame has ended and the Fieldbus line is free.

0 = Disable
1 = Enable

RX-OVR: Interrupt on receiver overrun. The receiver has detected an overrun error.

0 = Disable
1 = Enable

EOH: Interrupt on successful detection of end of header delimiter. Indicates end of reception of one Fieldbus Message.

0 = Disable
1 = Enable

RX-FCS: Interrupt on receiver FCS detection. Indicates that the FCS calculated for the received frame is correct.

0 = Disable
1 = Enable

DVAL: Interrupt on detection of start of header delimiter. Indicates that the start delimiter was detected and that the following Manchester signal is a valid Fieldbus data.

0 = Disable
1 = Enable

DPLL-LOCK: Interrupt on the end of Manchester phase locked loop. Indicates that a valid frame has ended. The DPLL-LOCK internal signal goes high when the FB2050 detects a valid Fieldbus Manchester signal and remains high until the FB2050 detects 6 missing transitions on the line. The falling edge of this internal signal causes an interrupt signal to the CPU

0 = Disable
1 = Enable

RDRF: Interrupt on receiver data register empty. Indicates that the receiver data buffer contains a new valid byte.

0 = Disable
1 = Enable

CONTROL_REGISTER_1

This register controls the basic operations of the FB2050 transmitter and receiver modules. During RESET this register is cleared.

	7	6	5	4	3	2	1	0
	X	X	X	X	FCS	H/F	EFC	X
RESET	0	0	0	0	0	0	0	0

EFC: Enable/ Disable Fieldbus Communication System (Transmitter, Reciever and Baud Rate Generator Modules)
0 = Disable
1 = Enable

FCS: Transmitter checksum generator
0 = Disable
1 = Enable

H/F: Half/Full duplex function selector
0 = Half duplex
1 = Full duplex

PROM_PAGE_REGISTER

The PROM page register is a 4-bit register that contains the PAGE_REGISTER PROM page number used to extend PROM address space. The value of this register is placed in pins PROMW[3-0] only when the processor accesses memory page 4000-7FFF. When any other memory address is accessed PROMW[3-0] points to # 0. During RESET this register is set to # 1.

Note: *The user should never write the value 0 into this register.*

	7	6	5	4	3	2	1	0
	X	X	X	X	PROMW3	PROMW2	PROMW1	PROMW0
RESET	0	0	0	0	0	0	0	0

RAM_PAGE_REGISTER

The RAM page register is a 4-bit register that contains the RAM page number used to extend the RAM address space. The value of this register is placed in pins RAMW[3-0] only when the processor accesses the memory page 0200-3FFF. When any other memory address is accessed RAMW[3-0] points to # 0. During RESET this register is set to # 1.

Note: *The user should never write the value 0 into this register.*

	7	6	5	4	3	2	1	0
	X	X	X	X	RAMW3	RAMW2	RAMW1	RAMW0
RESET	0	0	0	0	0	0	0	0

RECEIVER_BUFFER

The receiver data register can be read by accessing address BF00.

STATUS_REGISTER_1

This register contains all possible interrupt sources available in the FB2050. It is located at the address BF01. This register is recommended for polling operations.
After a RESET all flags will be cleared.

	7	6	5	4	3	2	1	0
	RDRF	DVAL	RX-FCS	EOH	RX_OVR	DPLL_LOCK	TMTR-ACT	TDRE
RESET	0	0	0	0	0	0	0	0

INTERRUPT_STATUS

The source of an interrupt is registered at this location. This register works in conjunction with the INTERRUPT_MASK and STATUS_REGISTER_1. If a source of interrupt is masked, its corresponding bit in the INTERRUPT_STATUS register will be 0. This register is cleared immediately after a read operation is performed. Its value should be stored in memory until all interrupt sources are properly processed.

During RESET all these flags are cleared.

IMPORTANT: *Never use INTERRUPT_STATUS for polling procedures; use STATUS_REGISTER_1.*

	7	6	5	4	3	2	1	0
	RDRF	DVAL	RX-FCS	EOH	RX_OVR	DPLL_LOCK	TMTR-ACT	TDRE
RESET	0	0	0	0	0	0	0	0

STATUS_REGISTER_2

This register contains additional status information for the receiver and transmitter modules of the FB2050. During reset its values are cleared.

	7	6	5	4	3	2	1	0
	1	AJ-FLAG	POLARITY	LA	1	TXS2	TXS1	TXS0
RESET	0	0	0	0	0	0	0	0

AJ-FLAG: Anti Jabber flag. Signals a transmitter error when the FB2050 has been using the transmission line for more than 131 ms (512 Fieldbus byte times).

POLARITY: Indicates the polarity of the received Fieldbus signal.
1 = Negative polarity
2 = Positive polarity

LA: Line Activity
1 = Line is busy
0 = Line is free

TXS2-TXS0: Transmitter State. These bits indicate the state of the transmitter submodule.

TXS2	TXS1	TXS0	Transmitter State
0	0	0	Idle
0	0	1	Send Preamble
0	1	0	Send Preamble
0	1	1	Send SOH
1	0	0	Send Data
1	0	1	Send FCS High
1	1	0	Send FCS Low
1	1	1	Send EOH

Table 4 - Transmitter States

Startup

1. Apply a low level hardware reset immediately after powerup.
2. Program desired values for CONTROL_REGISTER_1.
3. Program desired value for INTERRUPT_MASK.
4. Program desired values for RAM_PAGE_NUMBER and PROM_PAGE_NUMBER if applicable.

Transmitter Sub Module

1. Turn the transmitter on (dummy write to START_TRANSMISSION).
2. Write the first byte into the TRANSMITTER_BUFFER register.
3. Enable the processor's interrupt or polling system on TDRE.
4. Write the next byte of the message every time TDRE is high.
5. Finish the message by allowing a transmitter underrun. In this situation, the FB2050 will send the FCS (if enabled) followed by the EOH and enters the idle state.

If an anti jabber error has occurred the transmitter will be locked into the idle state until a hardware or software reset is performed. If hardware reset is not applicable:

1. Write a dummy value into TRANSMITTER_RESET.
2. Recover all values for CONTROL_REGISTER_1.
3. Recover all values for INTERRUPT_MASK.
4. Perform normal operations for the transmitter submodule.

Receiver Sub Module

The following steps describes the normal operation for the FB2050 Receiver Sub module:

1. Enable the processor's interrupt or polling system on RDRF.
2. Read the RECEIVER_BUFFER register every time RDRF is high.
3. If the received message contains an FCS, check the interrupt status register to make sure the FCS was correctly detected.

If a receiver overrun error has occurred it is important that the software recognized this occurrence and provide a proper reset sequence to the chip. The following steps should be performed.

1. Wait until STATUS_REGISTER_2 signals LA = 0.
2. Write a dummy value into RECEIVER_RESET.
3. Recover all values for CONTROL_REGISTER_1.
4. Recover all values for INTERRUPT_MASK.
5. Perform all normal operations for Receiver Sub module.

Reccomended Operating Conditions

Temperature	-40º to +85º C
Power	2.7V to 5.5V

Absoulte Maximum Ratings

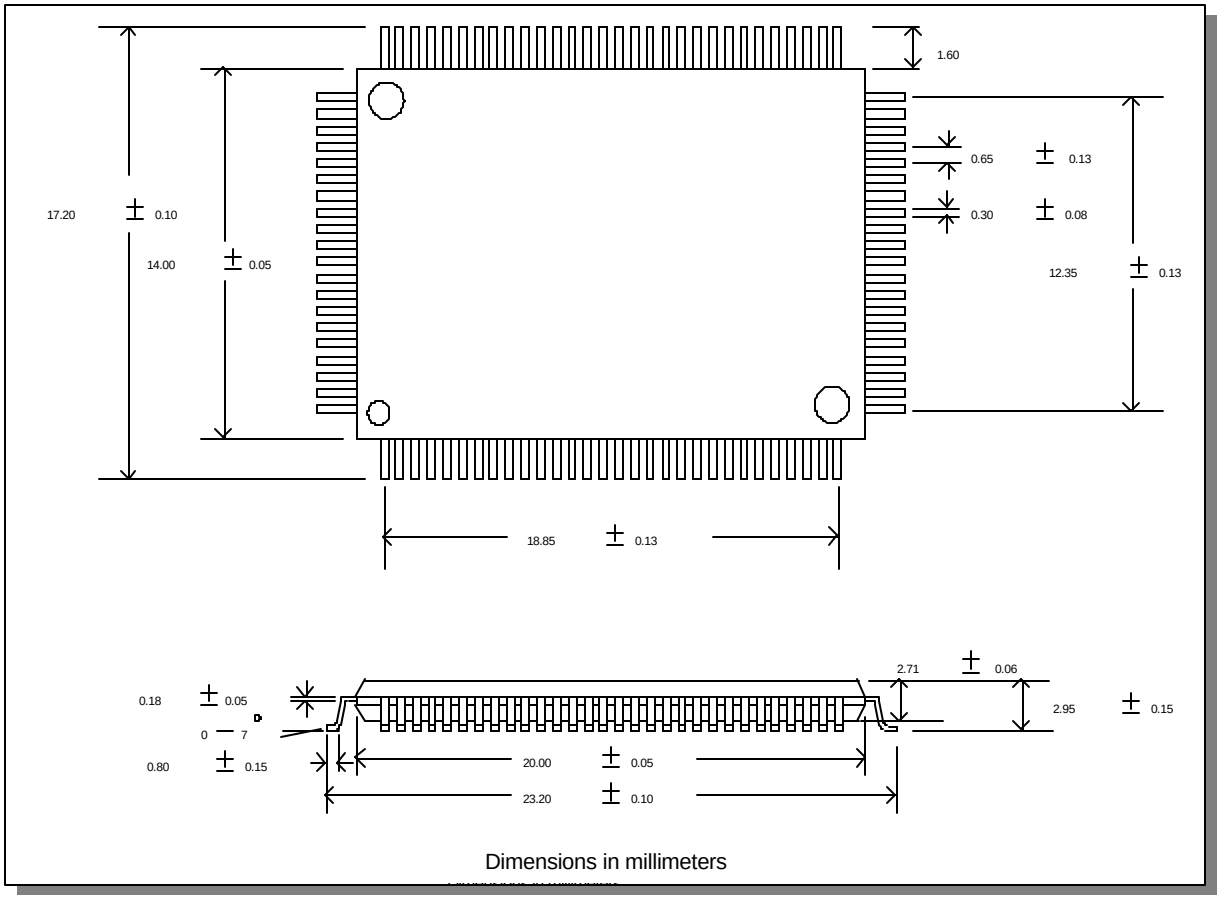
Vcc	DC Supply Voltage	-0.5 to + 7.0 V
Vin	Input Voltage	-0.5 to Vcc + 0.5 V
Vo	Output Voltage	-0.5 to Vcc + 0.5 V
Iik	Input Clamp Current	±20 mA
Iok	Output Clamp Current	±20 mA
Iok	Continuous Output Current	±25 mA
TSTG	Storage Temperature	-65 to +150º C

Package Thermal Characteristics

Pin Count	jc	ja (Still Air)	ja (300 ft/m)
100	13º C/W	55º C/W	47º C/W

Electrical Specifications

Parameter	Min.	Max
VOH	2.0 V	-
VOL	-	0.4 V
VIL	-0.30 V	0.80 V
VIH	2.00 V	Vcc + 0.3 V
Input Transition Time	-	500 nS
I/O Capacitance	-	10 pF
Standby Current (FIN = 0)	-	100 µA
Leakage Current	-10 µA	10 µA
Vcc (Power Supply)	2.7 V	5.5 V
Icc (Vcc = 5V; FIN = 5Mhz)		600 µA



Dimensions in millimeters

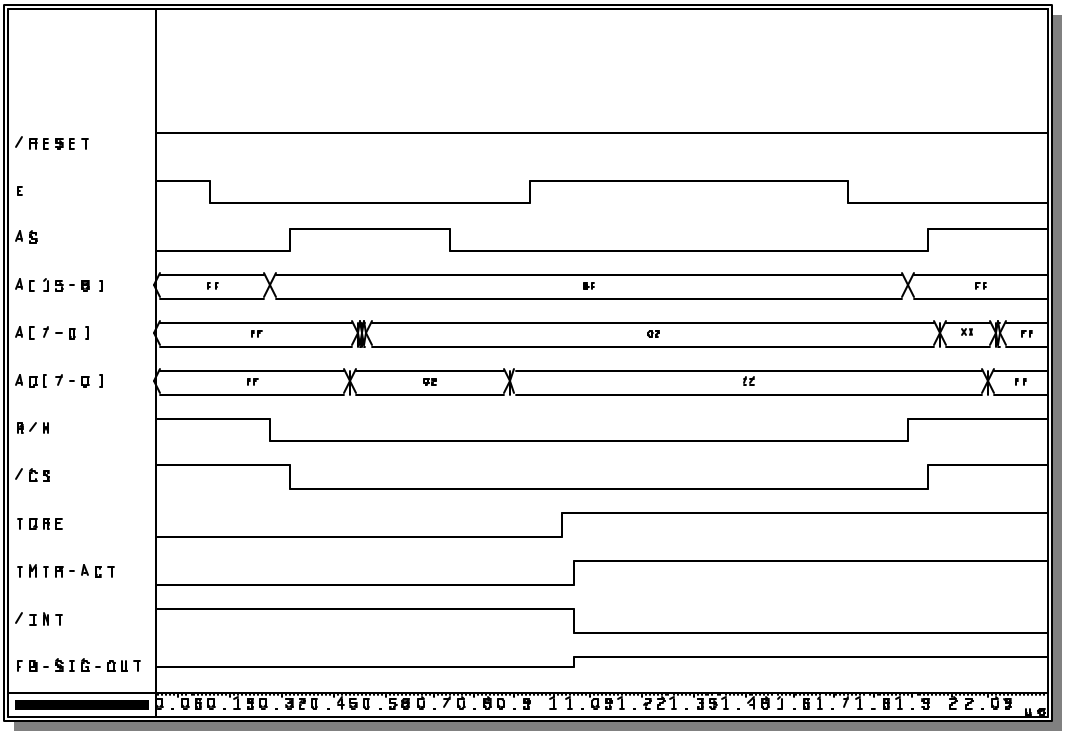


Figure 3 - Write to START_TRANSMISSION

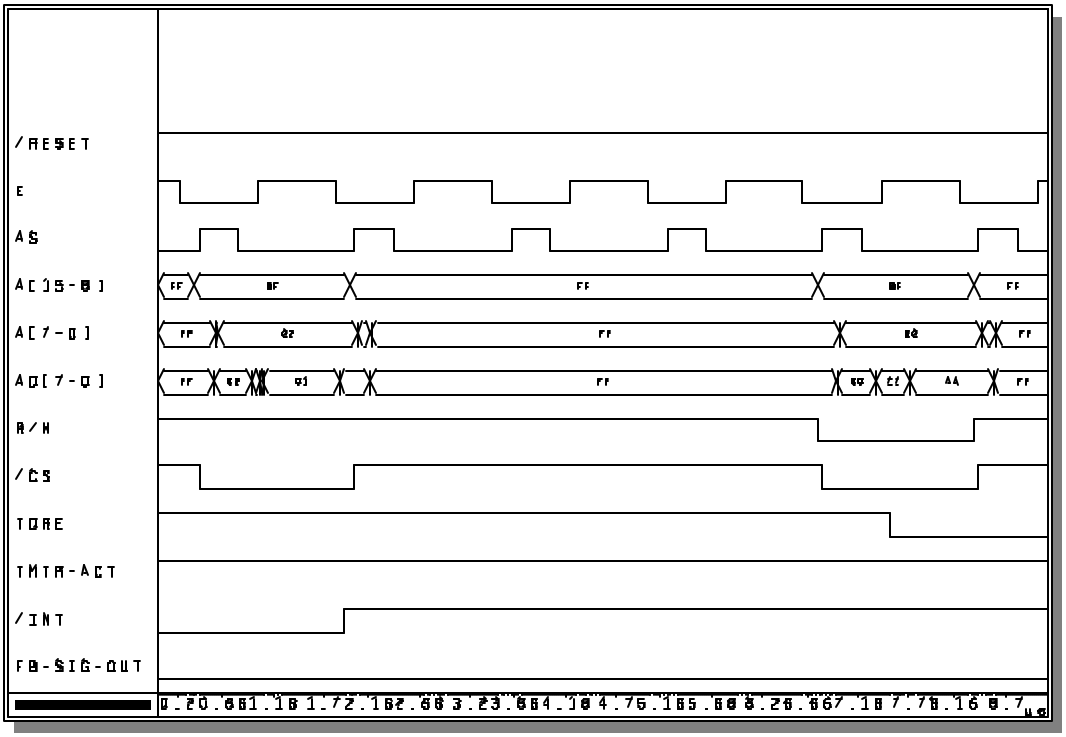


Figure 4 - Read INTERRUPT_STATUS and Write (AA) to TRANSMISSION BUFFER

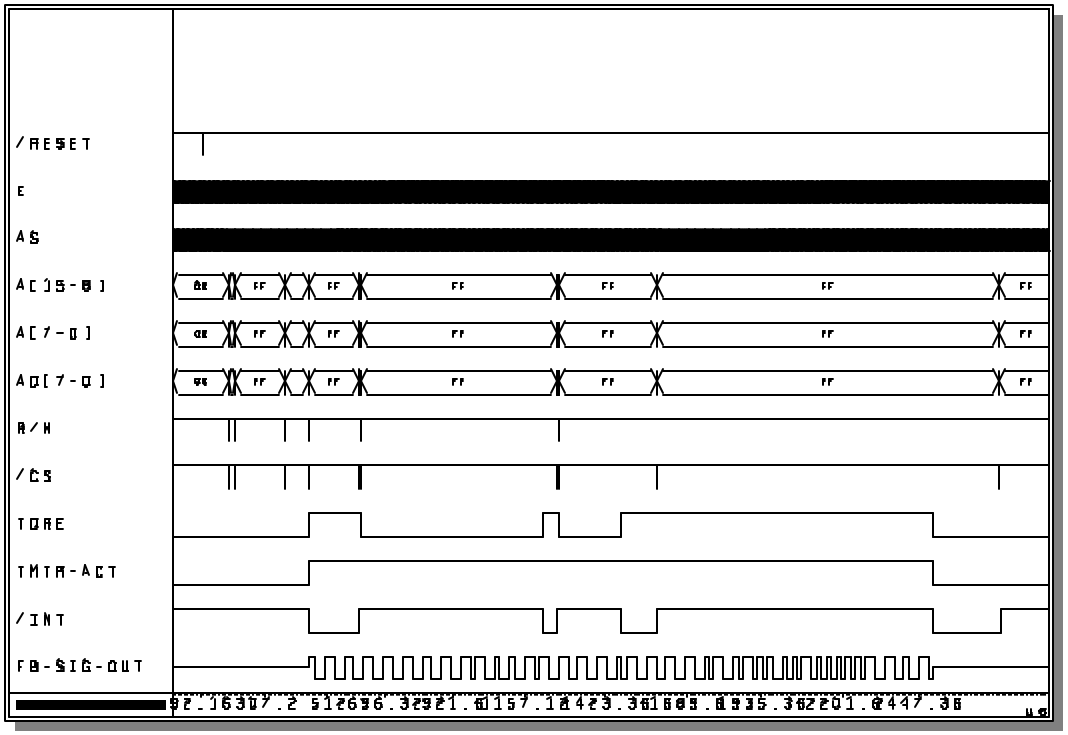


Figure 5 - Typical Transmission Procedure: 2 Bytes + FCS

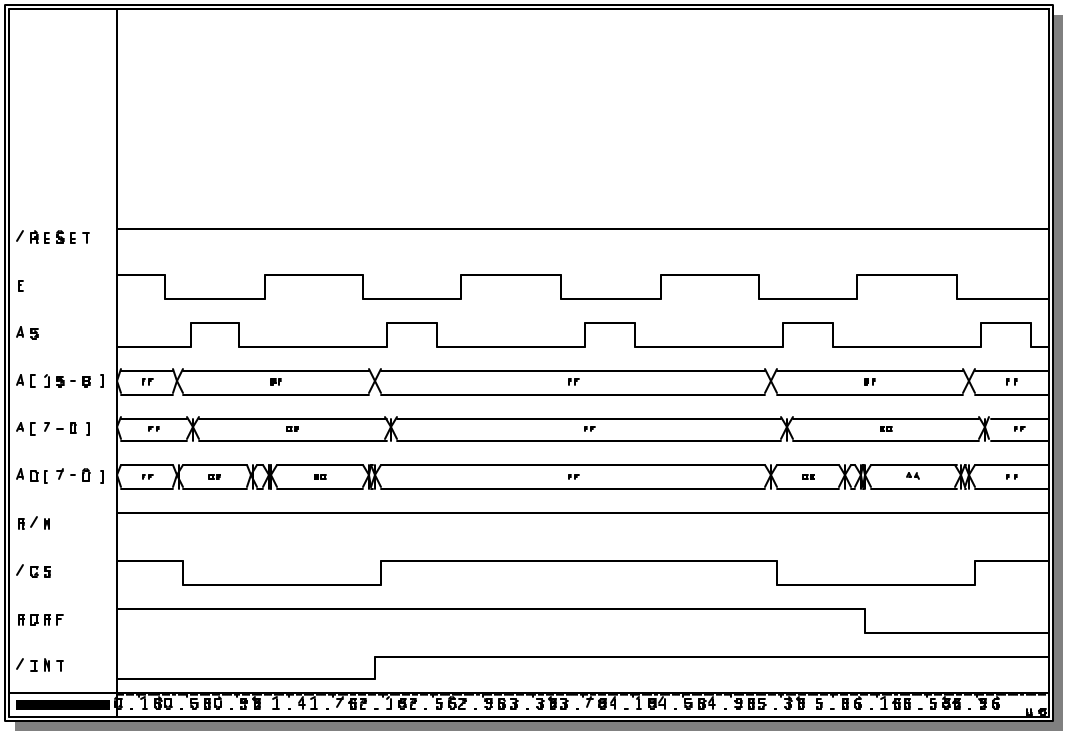


Figure 6 - Read INTERRUPT_STATUS Followed by Read RECEIVE BUFFER

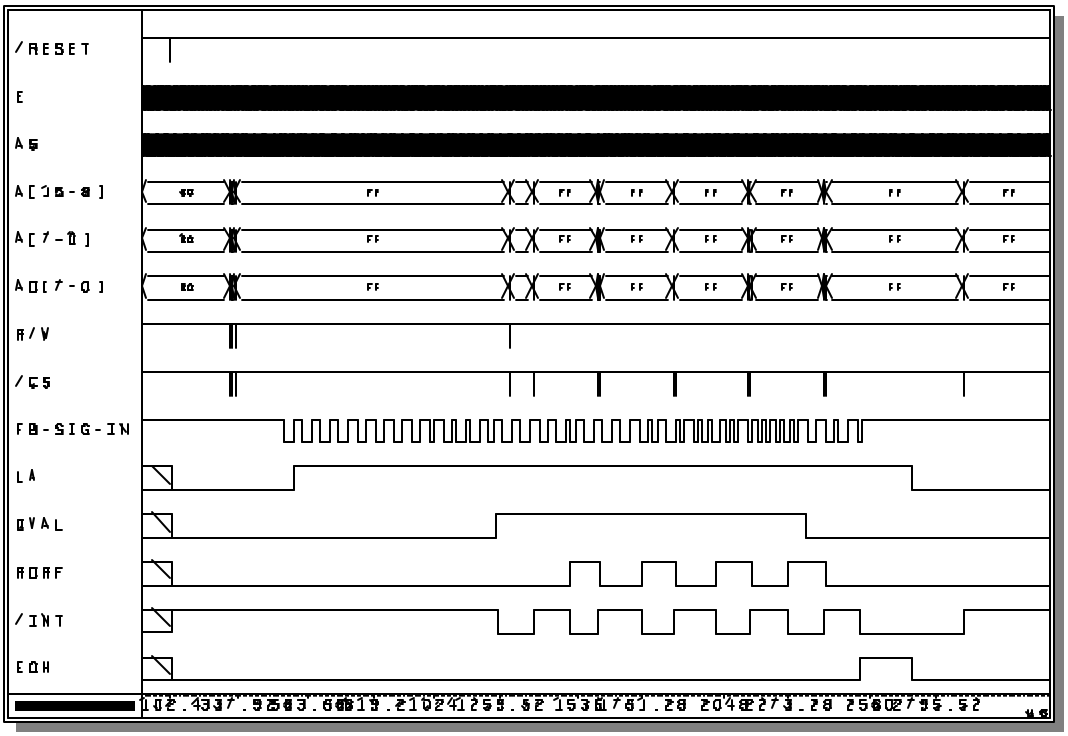


Figure 7 - Typical Reception Procedure - 2 Bytes + FCS

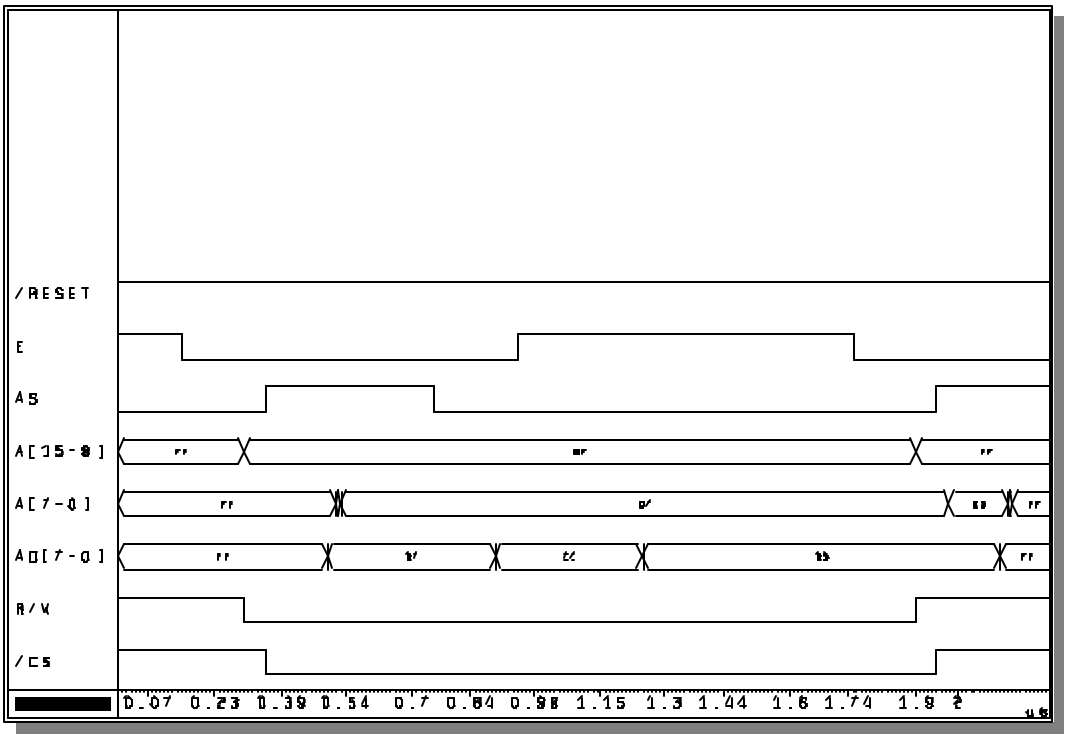


Figure 8 - Write (#03) to RAM_PAGE REGISTER

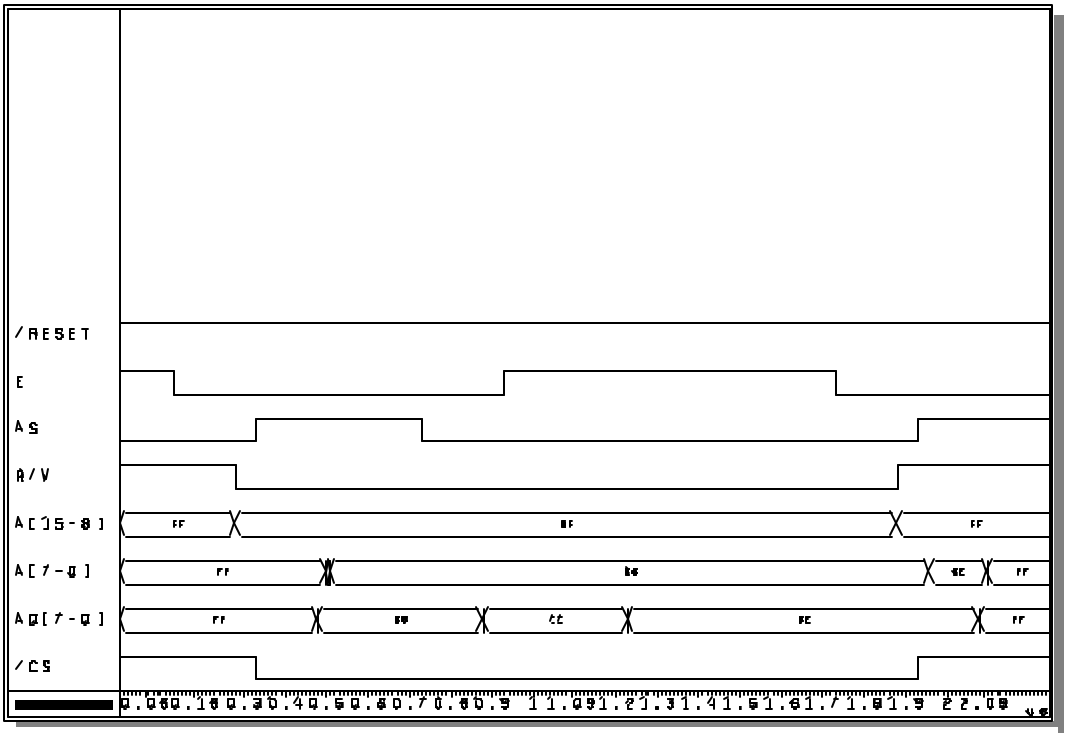


Figure 9 - Write (#OE) to PROM_PAGE_REGISTER

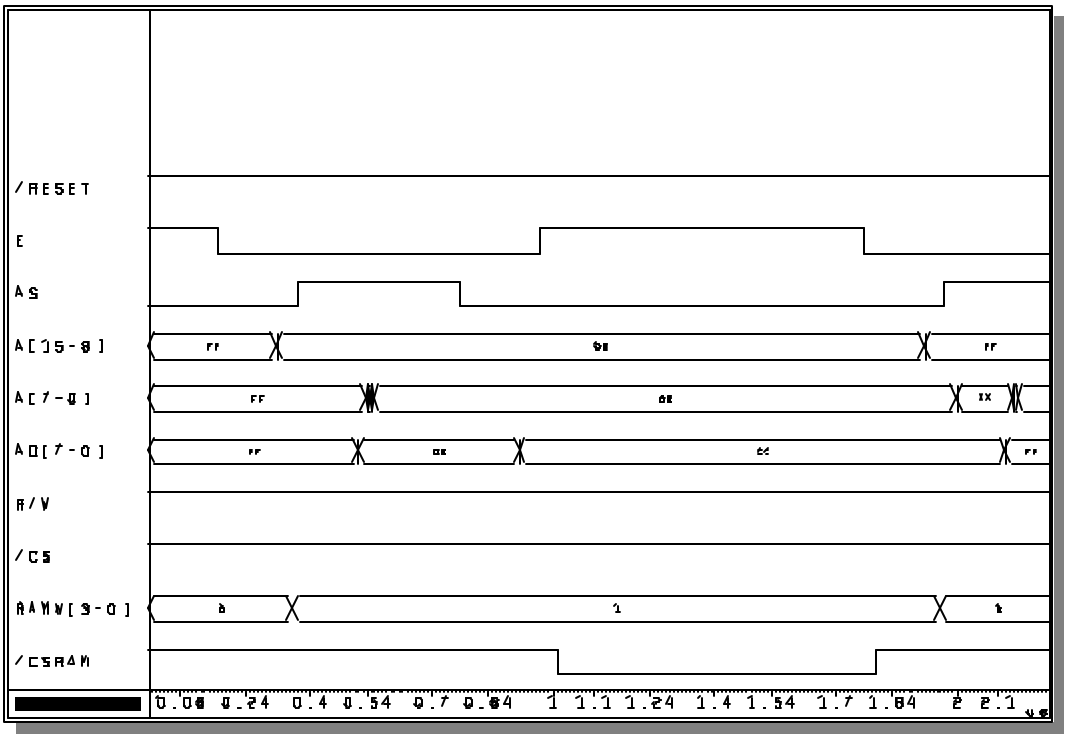


Figure 10 - Typical Read Operation From RAM Page #1

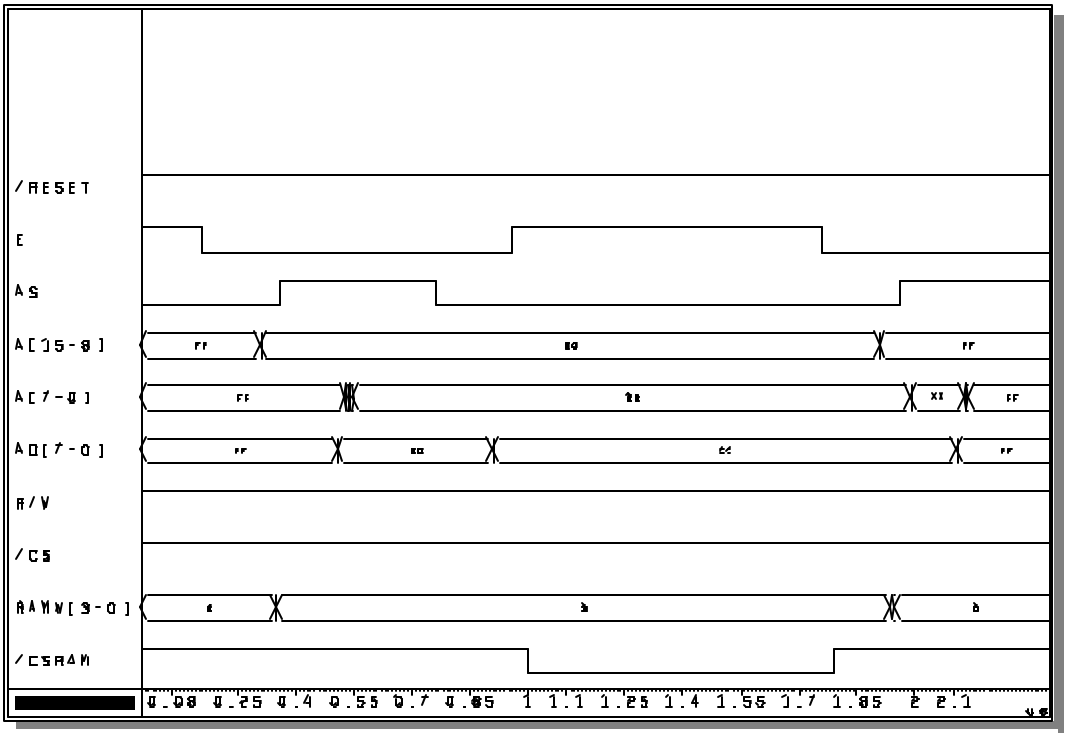


Figure 11 - Typical Read Operation from RAM Page

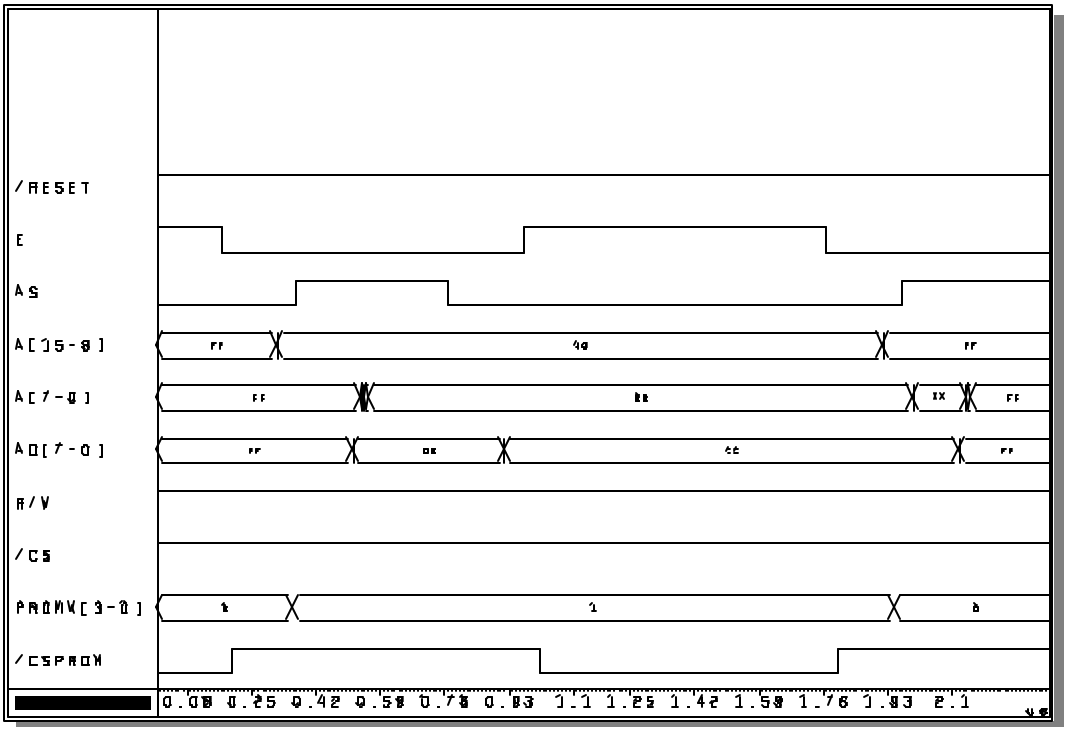


Figure 12 - Typical Read Operation From PROM Page #1

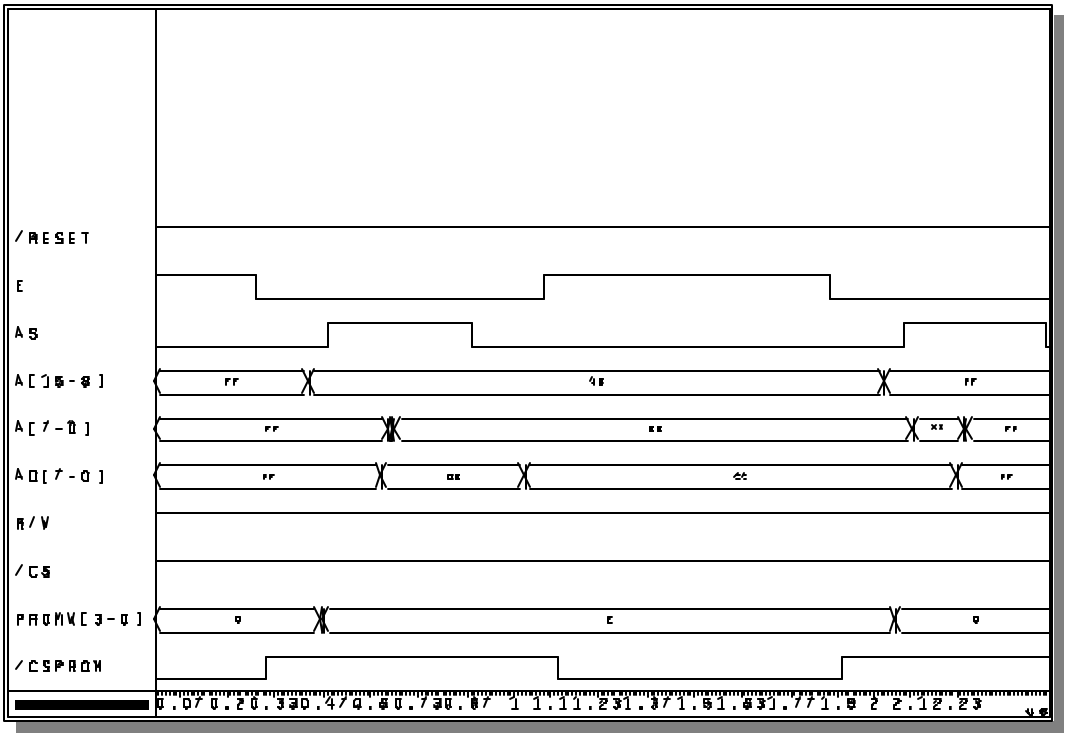


Figure 13 - Typical Read Operation from PROM Page #E

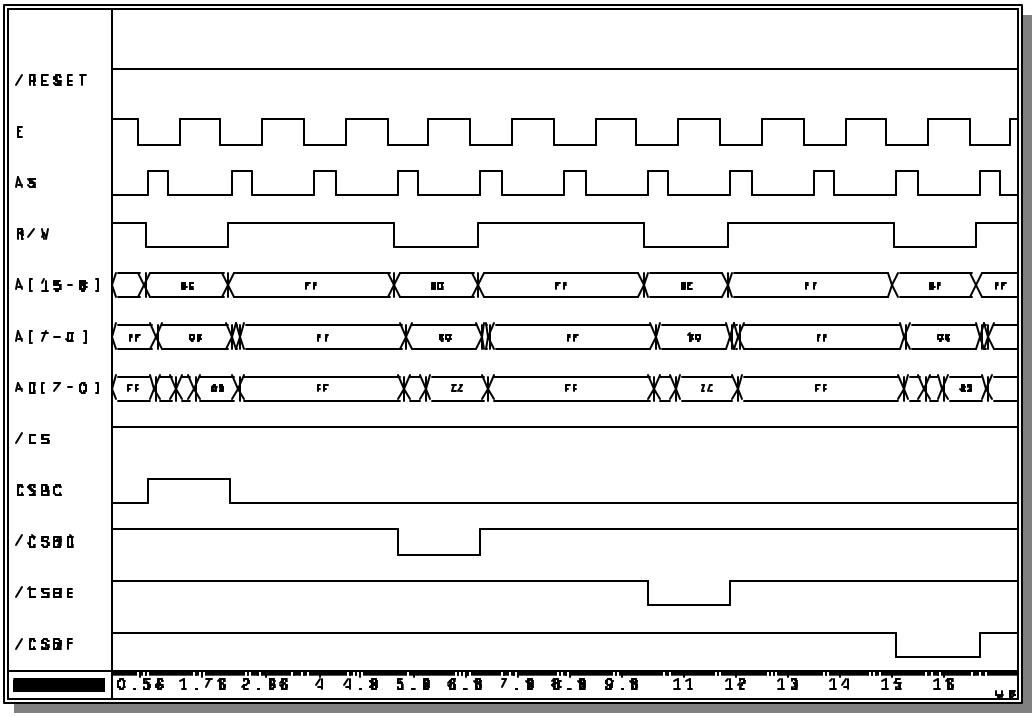


Figure 14 - Typical I/O Chip Selects

General Purpose Microcontroller and Microprocessor Interfacing

This section describes a general purpose microcontroller interface using the Smar Research FB2050™ Fieldbus Communication Controller. While a Motorola microcontroller is used in this example, the FB2050™ can be used with microcontrollers and microprocessors from most major vendors such as Intel and Zilog.

While specific needs and medium requirements vary between actual applications, the concepts and strategies described here cover the basic concepts necessary to implement control system designs based on the FB2050™

About the FB2050

The FB2050™ is an addressable microprocessor or microcontroller peripheral typically drawing only 0.6 mA. The FB2050™ handles all synchronization, encoding/decoding, check sum management, control, and status of a Fieldbus implementation. With the addition of a medium interface the FB2050™ creates fully compliant (IEC 1158-2 / SP50.02) microcontroller and microprocessor based nodes on a Fieldbus network.

Operating in full or half duplex mode the FB2050™ provides on chip address decoding as well as RAM and ROM page addressing to minimize component counts. The FB2050™ receiver features automatic Frame Check Sequence (FCS) detection and can perform automatic polarity detection and correction for incoming Manchester encoded data streams. The transmitter automatically generates FCBs under software control. The FB 2050 operates in both modes at a 31.25 KHz data rate over wires, twisted pair, coax, or fiber optic mediums.

Designing Fieldbus interfaces using the FB2050

To design a Fieldbus node using the FB2050 eight stages must be implemented:

Various tables and schematics provided in this document describe d these stages in more detail.

- clocks and timing
- microcontroller interfacing
- transmit drivers
- transmit wave shaping filter
- buffered voltage reference
- receive bandpass filter
- voltage limiter
- isolation circuitry

Clocks and Timing

The FB2050™ can accept either a 625 KHz input clock or a 1.25 MHz input clock with the same 0.2% accuracy . The choice is provided to help minimize component counts.

In the application a 5 MHz crystal oscillator divided by a dual flip flop, (HC74) is used to generate a 1.25 MHz clock. CLKSEL is tied high selecting the 1.25 MHz input clock for the FB2050™. Using a third flip flop,the 625 KHz clock can be generated and CLKSEL tied low.

A 156.25 KHz clock is also provided. This is a base clock used internally for synchronization and can be used externally for general purpose synchronization and timing.

Microcontroller interfacing

An active low RESET* pulse can be configured as a self standing power up reset using a resistor and capacitor, or can be patched along a reset chain from the system. The reset pulse should be 200 nsec or greater in duration to assure a valid reset that is asynchronous. In this application the reset pulse is from the host system.

Although the FB2050™ can decode addresses directly from the microcontrollers address bus and control signals, this application assumes I/O or memory mapped decoding for the FB2050™ has already been provided. An active low Chip Select (120 nsec or longer) from the decode section enables the FB2050™ on the /CS line.

When selected, the FB2050™ responds to addresses on the C0-C2 lines to determine the internal register to read or write to depending on the state of the R/W line. A logic 1 on the RD/WR line implies a read and a low implies a write. The address on C0-C2 allow access to transmit/receive buffers, control/status registers, page registers, and internal resets (Table 5).

The E clock input is used to synchronize reads and writes of the FB2050™ with a Motorola based microcontroller and should be connected to the Eclock line of the processor. If a none Motorola microcontroller is used, this line can be generated by NANDing an active low read or write signal to assure that the Eclock line is logic 1 when the read or write is in progress. In this case, the active low read signal would also tie to the RD/WR line on the FB2050™.

The E clock can be tied to VCC if the timing characteristics follow the specifications in figures 15 and 16. Figure 15 illustrates the read cycle timing and figure 16 illustrates the write timing relationships. The important signals relationships are the ADDRESS BUS to RD/WR, RD/WR to chip select, and chip select to the DATA BUS. With synchronized operations the Eclock need not be connected since internally the FB2050's chip select line will alternately perform the internal clocking.

C2	C1	C0	R/W	Operation (synchronized with E)
0	0	0	0	TRANSMITTER_BUFFER
0	0	1	0	TRANSMITTER_RESET
0	1	0	0	START_TRANSMISSION
0	1	1	0	RECEIVER_RESET
1	0	0	0	INTERRUPT_MASK
1	0	1	0	CONTROL_REGISTER_1
1	1	0	0	PROM_PAGE_REGISTER
1	1	1	0	RAM_PAGE_REGISTER
X	0	0	1	RECEIVE_BUFFER
X	0	1	1	STATUS_REGISTER_1
X	1	0	1	INTERRUPT_STATUS
X	1	1	1	STATUS_REGISTER_2

Table 5

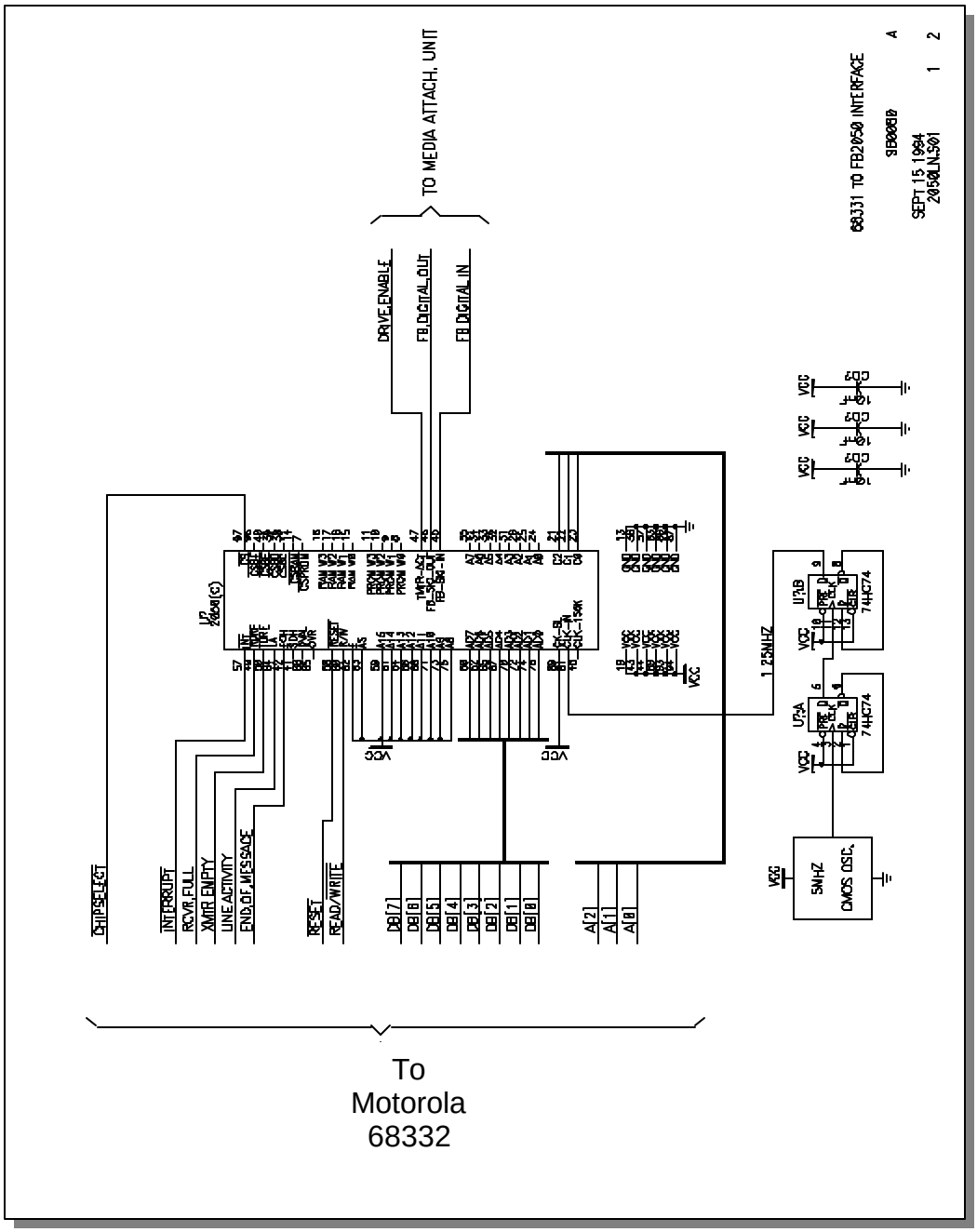


Figure 13 - Microcontroller Interfacing

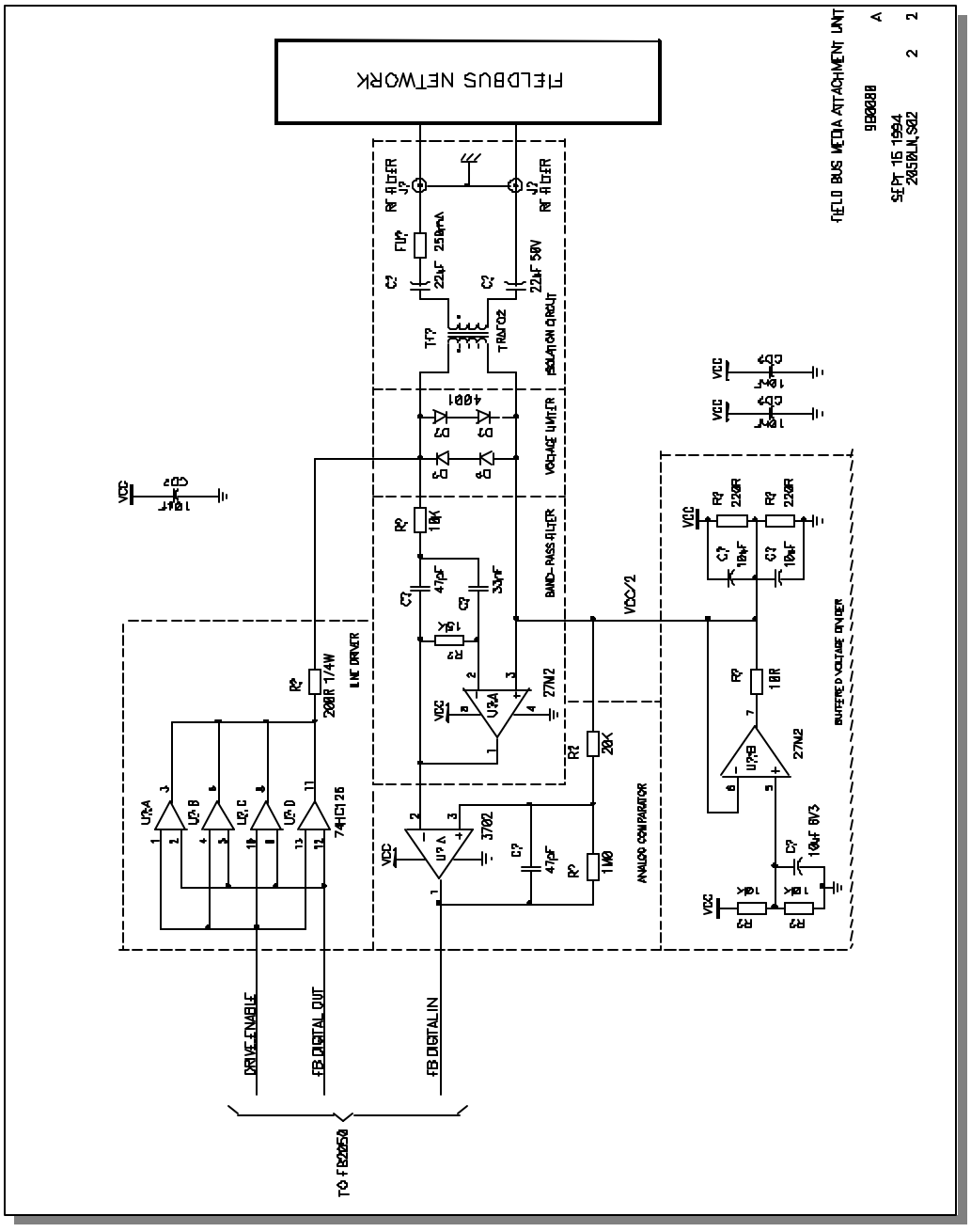


Figure 14 - Analog Media Interfacing

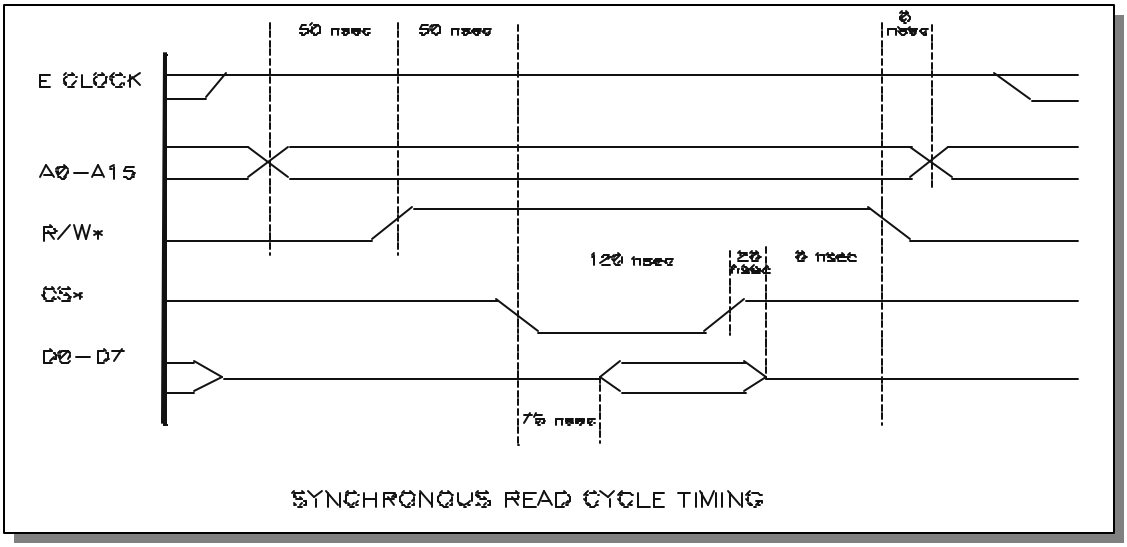


Figure 15 - Synchronous Read Cycle Timing

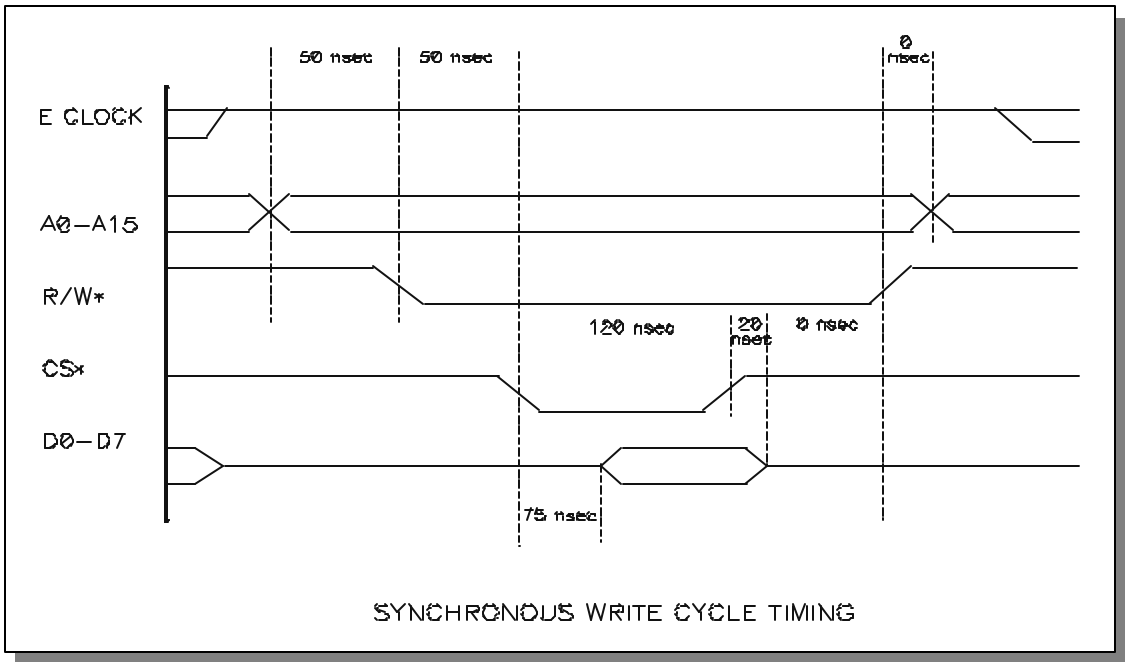


Figure 16 - Synchronous Write Cycle Timing

The FB2050™ generates an active low interrupt when tripped by an unmasked interrupt source. Masking occurs by writing into the interrupt mask register to enable and disable specific interrupt sources. The interrupting source can be determined by reading an internal interrupt status register or read by a microcontroller status port.

Key status signals, although available by reading internal status registers, are brought out to external signal lines on the FB2050. These are receiver full (RDRF), transmitter empty (TDRE), line activity (LA), and end of message (EOH). Although a single interrupt system can be used to control and access the FB2050 these lines can be brought out to separate interrupts to increase performance and throughput. Instead of have one unified interrupt routine that adds overhead to identify the source a unique interrupt for these conditions can quickly service the FB2050™. The line activity signal (LA) can also be used to drive the interrupt driven capture register for synchronization of framing on the bus.

Note: *To connect directly to the microcontroller use the AS (address strobe) input as an active high pulse which latches the valid low order address from the multiplexed data/address bus (AD0-AD7). The latched low order address bus is provided on the A0-A7 outputs for reduced chip count when interfacing to external memory or peripherals.*

When addressed and selected by the microcontroller, the internally latched low order address as well as the high order address bus (coming in on A8-A15) are used to generate decoded selects which are output from the FB2050. The / CSPROM pin strobes active low when addresses between 4000-7FFF and C000-FFFF are accessed. This can be used to select external code PROM for the microcontroller.

Also generated and output is the active low strobed /CSRAM signal which allows external RAM selects for addresses 0200-3FFF and 8000-AFFF. This is useful for connecting external RAM for general purpose use without additional logic.

In addition to the ROM and RAM block selects, the FB2050™ provides paging control lines for banked external memory. In this case the PROMW(0-3) output lines present the contents of the internal ROM page register when addressed accesses between 4000-7FFF occur.

Likewise, the RAMW(0-3) output lines present the contents of the internal RAM page register when accesses between 0200-3FFF occur. In both cases, these lines are used to map in external memory blocks or pages into a fixed address space and can logically extend the otherwise limited address range of the microcontroller.

Other general purpose decoded signals provided by the FB2050™ include the CSBC, /CSBD, /CSBE, and /CSBF. The CSBC generates an active high pulse when addresses between BC00 and BCFF occur. The /CSBD line provides an active low strobe when addresses between BD00 and BDFF. The /CSBE and /CSBF lines strobe active low when addresses between BE00-BEFF and BF00-BFFF respectively. Note, you can use the /CSBF line to select the FB2050™ itself, eliminating an additional decode section to minimize component counts.

Transmit Drivers

The digital transmitter output from the FB2050™ does not supply enough current to drive the line directly and must be buffered to increase the signal strength for transmission. In our example, we use a quad three state buffer (the 74HC126) paralleled to increase output current capacity. The tristate control line can be tied to the transmitter activity pin on the FB2050.

Note: *it is important to provide a large capacitor in close proximity to the HC126. Since the output signal will be AC coupled to the Fieldbus network, you want to provide a clean, ripple and noise free power supply to the HC126. This helps guarantee that no conducted noise escapes from the Fieldbus interface to the Fieldbus lines. In our application we use a 10 uF capacitor. Depending on your choice of drivers and power supply, you may need a larger capacitor and/or an LC decoupling circuit to guarantee clean power into your driver section.*

Transmit Wave Shape Filters

The transmit wave shape filter serves to unsharpen the digital transmissions of the output waveform. An output wave shaping filter is not needed in all cases if the medium can accept square waves without emanating unacceptable levels of EMI/RFI or noise. Otherwise, the wave shaping filter should be used to smooth the transitions between logic 0 and logic 1.

Transmit Driver And Wave Shape Filter Application

When using a waveshape filter, it is important to guarantee the best phase relationship of filter response. This invariably helps assure that the timing of the transmitted signal can accurately be reproduced at the receiving end. With Manchester encoded data, the edge relationships play a big part in recovering the data clock so non-symmetrical timing can lead to cumulative errors with long data streams.

In this application, the characteristics of the isolation transformer and coupling capacitors are used to smooth the output waveform. This simplified approach is sufficient for most direct wiring, short haul, low to medium noise environments.

A simple form of output wave shape filter is an integrator. A capacitor across the data line will exhibit a charge up and discharge time effectively smoothing the transitions on the line. Although the waveform approaches a trapezoidal wave, timing relations are preserved and within the Fieldbus specification for transmitted waveforms .

A more elaborate active wave shaper can be employed as well. Here current mirror or quadrant OP AMPs can be used to shape the transitions in a more precise way. It will inevitably depend on your choice of medium to determine your exact needs for transmit wave shaping filters.

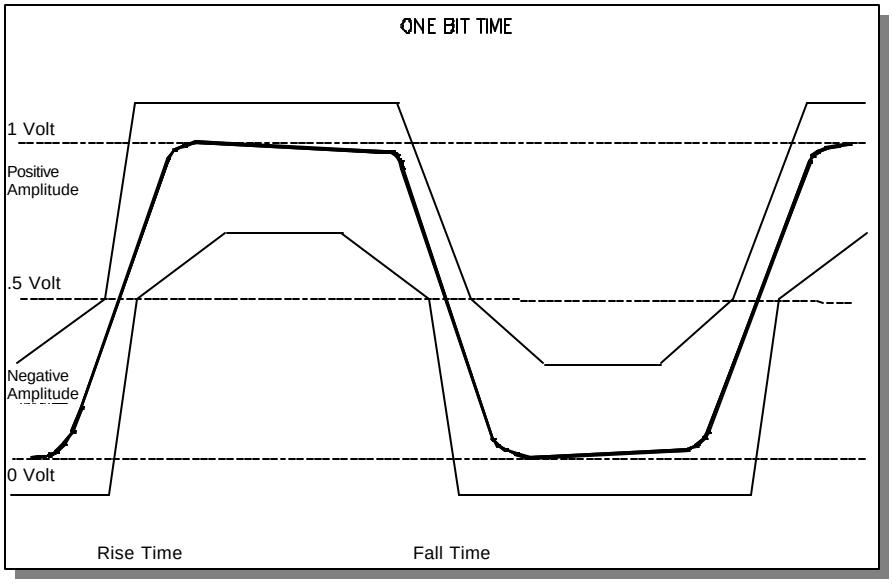


Figure 17

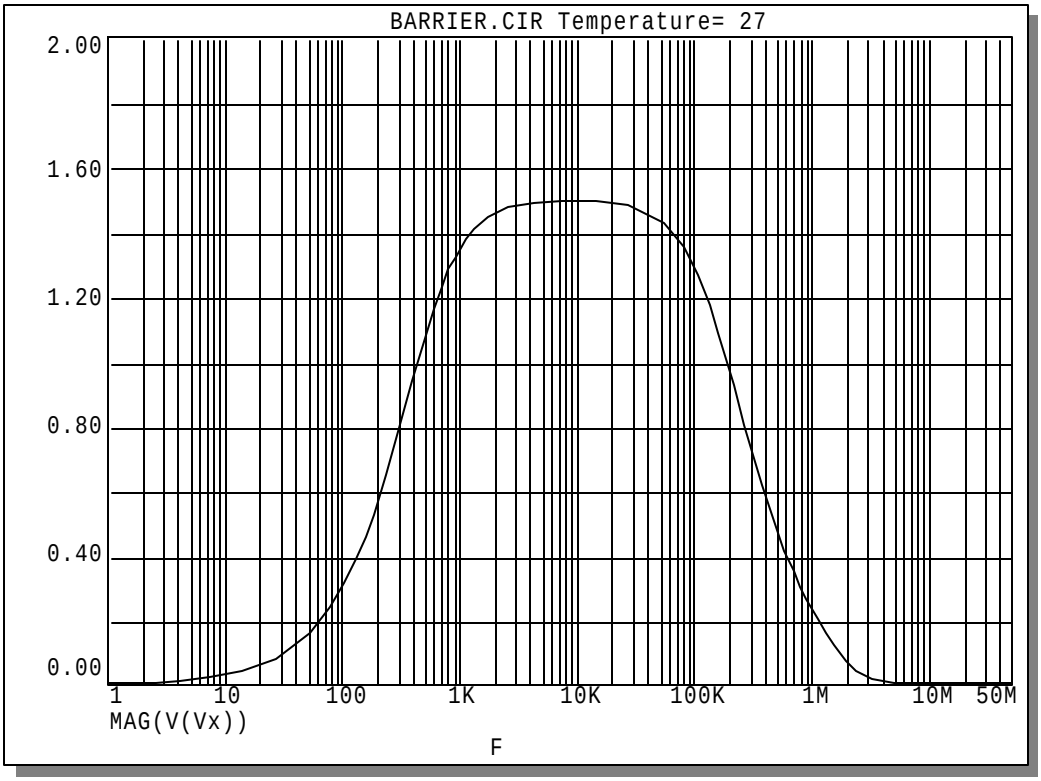


Figure 18

Buffered Voltage Reference

As our design uses a single polarity power supply, all signals are referenced around a VCC/2 point. To obtain this VCC/2 point, we need a clean and stable voltage reference. In our example, we set up a resistive voltage divider with a parallel capacitor to further stabilize our input reference.

A unity gain non inverting OP AMP serves to buffer the reference and provide a low output impedance to drive all referenced points. Another voltage divider with low impedance is connected to the OP AMP output along with some large parallel capacitors. This will physically drive enough current to make this reference relatively immune to any local noise. Since this voltage reference is used for receive data filtering and squaring, any noise or shift in reference level can shift the timing relationships of received data streams. This is undesirable since the timing relationships are required to regenerate data and clock for receive data.

Receive Band Pass Filter

The receive band pass filter is important to eliminate out of band noise and interference. It is also responsible for assuring uniform relatively flat phase response over the 15 to 32 KHz band to assure accurately reconstructed timing signals for data and clock recovery. The receive band pass filter also presents clean squared signals to the FB2050™ in digital form.

In the example application, a single stage OP AMP bandpass filter feeds a Schmidt triggered comparator with hysteresis. Although the Manchester data will ideally present 15.625 or 31.25 KHz pulses, the transitional responses needed to recover the signal span a wider band. The low frequency cutoff is dependent on line characteristics. The high frequency cutoff should be lower than any switching noise that can be induced from switching power supplies or other local oscillators.

The filter has a low frequency cutoff of 8 KHz with an active signal band between 8KHz and 40 KHz *(see Figure 18)*. This is the frequency range which we want to optimize phase delay characteristics around *(see Figure 19)*. The high frequency cutoff falls out around 110 KHz. The Q is 1.0.

The output of the filter is fed into a comparator biased as a Schmidt trigger with hysteresis. The feedback R/C values determine the hysteresis characteristics. The output is a clean square wave in digital format.

For both the input bandpass filter and the comparator, a voltage reference of VCC/2 is used to set a centerpoint. Because this design uses a single power supply OP AMP, the voltage reference serves to center the received waveform AC within the active range of operations for the OP AMPs. The comparator functions as a zero cross detector for the AC waveform in.

The VCC/2 is generated by a resistor divider feeding a unity gain non inverting OP AMP. The OP AMP output feeds the filter and comparator as well as biases the isolation transformer.

Voltage Limiter

On the FB2050™ side of the transformer, a double diode hard limiter is used to guarantee the signal does not exceed 1.25 V peak to peak over Fieldbus. Your gain calculations for the output transmitter circuitry and receive filter circuitry should be centered around a 1 volt peak to peak signal level over the Fieldbus media.

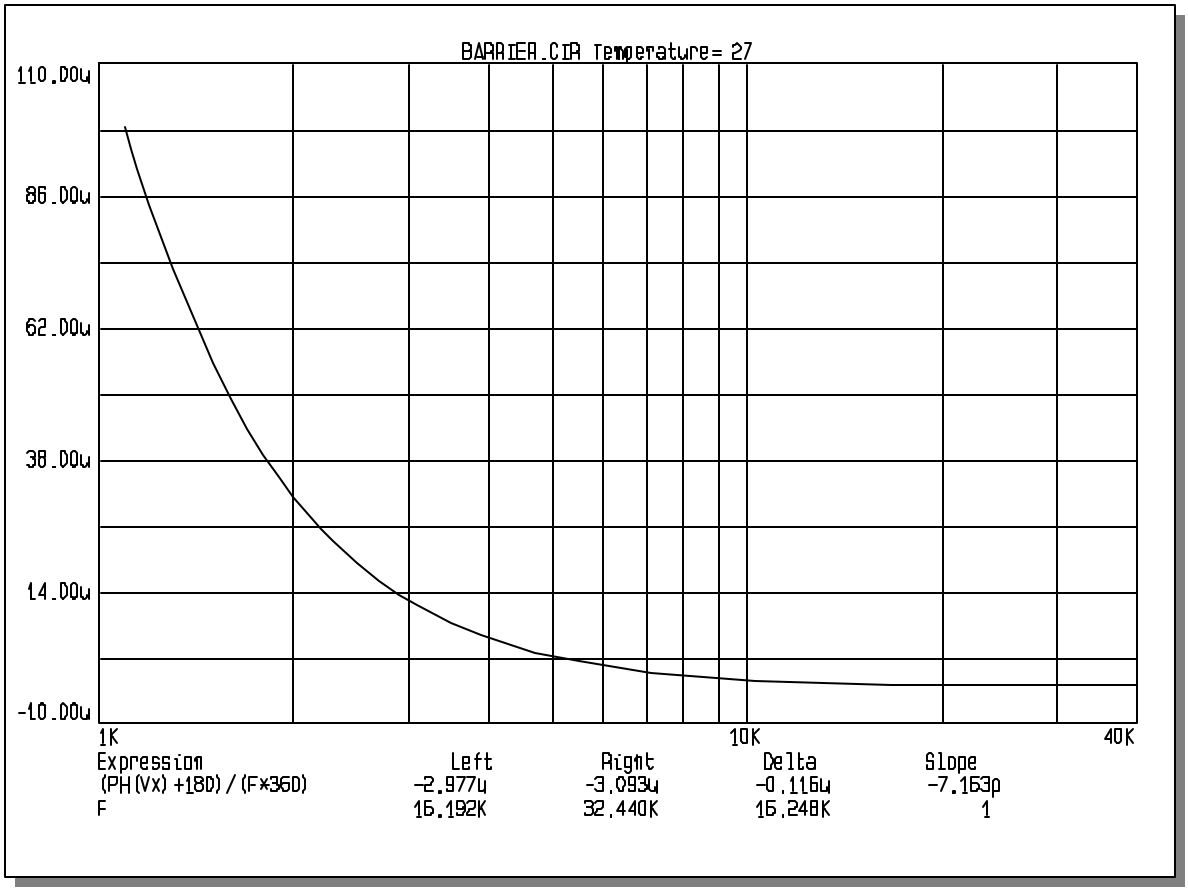


Figure 19

Isolation Circuitry

The media interface circuitry will vary depending on your media characteristics. In our case, an isolation transformer is used electrically isolate the interface toThe transformer has a 1 to 1 turns ratio.

On the isolated side of the transformer, coupling capacitors allow data to pass through and block DC levels on the Fieldbus network from interfering with the transformer. If this interface were drawing power from the Fieldbus media, or, supplying power to it, this coupling scheme would be different.

In addition, a fuse is placed in series with the isolation transformer windings to guard against excessive power surges or massive faults. This is set a 250 ma which is more than any valid signal would ever be presented to the transformer.

The VCC/2 biasing of the primary side of the isolation transformer centers the output waveform. In this way an effective Non Return To Zero (NRZ) waveform is fed to the primary assuring a symmetrical waveform for transmission and reception.

In addition, RF blocking circuitry is used to feed a signal through your chassis. The value and specifications for the RF filter will depend solely on your implementation and is mostly influenced by the type of enclosure you are using and the levels of noise within and external to your enclosure. This last stage should be chosen specifically for your design.

Note: *Media characteristics will ultimately depend on the choice of media interface being used. The characteristics of the enclosure will determine the type of feedthrough capacitor or RF filtration needed.*

The FB2050 contains all of the circuitry needed to create a microcontroller or microprocessor based node on a Fieldbus network. The inherent flexibility helps minimize external components necessary to implement a fully compliant Fieldbus interface. Additional features are also provided to allow expansion of buffer memory and code memory for added integration. The SMAR FB2050 is an ideal choice for designers implementing Fieldbus designs.

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