

Fieldbus Communications Controller FB4050 **DataSheet**



Asynchronous Bus (READY Methodology)

Features

- Software controlled transmitter FCS generation
- Transmitter jabber inhibit circuitry
- Maskable Multisource Interrupt Structures reduce software response times
- Timers available for Data Link Layer timing
- Built-in:
 - Floating Point Coprocessor Unit (FPU) increases processing performance
 - Manchester encoder/decoder
 - two channel DMA controller
 - LCD driver for up to a 160-segment display
- Automatic :
 - LCD Position Orientation and Segment Reorganization allows multiple display positions
 - polarity detection and correction
 - receiver frame check sequence (FCS) detection
 - message type and address recognition
- Simplifies design, shortens development schedule, saves on parts and lowers cost of manufacturing
- Conforms to Fieldbus H1 Device standards and Profibus PA
- Designed for easy integration with Mitsubishi M16 and Intel 80186/80188 microprocessors

General Description

The FB4050 Fieldbus Interface and Controller conforms to the IEC 1158-2 standard, Fieldbus Physical Layer Definition. It provides a high level Master or Slave Fieldbus interface with both embedded and host microprocessors.

The FB4050 contains Manchester data encoders and decoders on chip. Only a medium interface and external filters are needed to connect to a Fieldbus system. The FB4050 automatically detects and corrects polarity reversals on improperly wired connections, automatically checks the Frame Check Sequence (FCS) for received data packets, and generates FCS for transmitted data packets when enabled by a software control command.

Frame status is available by software control commands in internal status registers. A Jabber Inhibit function helps assure a transmitter does not disable the communications network by transmitting beyond a specified time.

To accommodate high throughput, the FB4050 Controller features an on-chip two-channel Direct Memory Access (DMA) circuit. When the DMA is configured, data blocks (frames, buffers) can be sent and received to and from the system memory without significant byte transfer overhead. When interfacing to the microprocessor, the FB4050 uses the PO_HOLD signal to request the microprocessor to go into a wait state and the microprocessor uses the PI_HLDA signal to acknowledge the request until the DMA access cycle has finished. When the FB4050 has finished its DMA cycle, the PO_HOLD signal will return to its inactive state (high) and the CPU will return PI_HLDA to its inactive state. In the cases where multiple FB4050's are used

in the same device, the PO_HOLD signals can share the same signal path to the CPU. However, the PO_HLDA signal from the previous FB4050 must be connected to the PI_HLDA of the next FB4050. This effectively forms a "daisy-chain" that will pass along the signal to each controller.

In-the-field readable output is achieved with an integrated three-ledger 160-segment display driver. This LCD driver can be used to output device readings and calculations to various types of LCD's in the field. The display frequency can be modified by software control commands to various divisions of the input clock frequency. The display module has the added capability of detecting the LCD position and reorganizing the data segments appropriately to accommodate for various LCD rotations suited to each device location.

A 32-bit floating point unit is also incorporated into the FB4050. This FPU can perform the following operations:

- Addition
- Subtraction
- Multiplication
- Division
- float to integer conversion
- integer to float conversion
- Clear contents of accumulator A.

The inclusion of the FPU in the FB4050 improves performance by allowing the microprocessor to execute other tasks while the FB4050 performs the floating point calculations. The FPU operation frequency can be modified by software control commands to various divisions of the input clock frequency.

General Description (continued)

To reduce software overhead, the FB4050 Controller provides detection of the Frame Control character. Depending on the value received a test for equality for 8 bit, 16 bit or 32 bit addresses is made by comparing the received address with a table of addresses contained in memory. The search for a match is automatic. An interrupt is generated when a match occurs. Only one address loads into an internal register(fb_nodeid) for an 8 bit compare. Address fields in memory support a variable number of 16 bit and 32 bit addresses. Frame Control message types that do not require address recognition are also detected and can generate an interrupt.

The FB4050 has a flexible interrupt structure. A single interrupt will cause the host to read internal status registers to determine the source. All interrupt sources are maskable and identifiable. An interrupt is generated by a number of

conditions or by any of the controllers' three timers. The Timer Module provides octet, 1/32 millisecond and millisecond timing references. All of these conditions are also maskable. When only one FB4050 is used in the device, the PI_INTR pin is connected directly to the CPU to monitor external interrupts. In the cases where multiple FB4050's are used in the same device, the PO_INTR signal from the previous FB4050 must be connected to the PI_INTR of the next FB4050. This effectively forms a "daisy-chain" that will pass along the signal to each controller. The PO_INTR and PI_INTR signals are active level low, effectively being active for the entire duration the signal is low and not just on the falling edge. Because of this, it is required to manually reset the interrupt after the interrupt service routine is completed; otherwise the service routine will run indefinitely.

Pin Configuration



Figure 1 - Pin Configuration

FB4050 - Pin Configuration

Pin Descriptions

The FB4050's pins are divided into six major groups: Clocks Interface, Fieldbus Interface, Memory/Microprocessor Interface, LCD interface, Sensor Interface and Power Interface.

Clock Interface Pins

<u>PIN NAME</u>	<u>PIN#</u>	<u>FUNCTION</u>	<u>REMARKS</u>
PI_BCLK	123	System clock that synchronizes operations to the host microprocessor.	Provided by the host microprocessor clock and applied by the FB4050 for all memory operations.
PO_CLK125	26	A 125 KHz general purpose clock signal. Applies for any external general purpose function.	Internally generated.

Table 1 - Clock Interface Pins

Fieldbus Interface Pins

<u>PIN NAME</u>	<u>PIN#</u>	<u>FUNCTION</u>	<u>REMARKS</u>
PI_PHPDU	31	Fieldbus receive data signal.	The signal provides digital data in Fieldbus Manchester format from the media interface.
PO_PHPDU	35	The transmit data signal. tri-State when idle.	Data is Fieldbus Manchester encoded and will be conditioned by the media interface.
PO_TXEN	34	Enables external drivers depending upon the media interface.	An active high signal indicates that the transmitter is active.
PO_TDRE	33	An active high signal from the FB4050 indicates that the transmit data register is empty and a Fieldbus data byte can be transmitted.	Also can be determined by reading the internal interrupt status register.
PO_RDRF	32	An active high signal from the FB4050 indicates that the receive data register is full and can be transferred.	Also can be determined by reading the internal interrupt status register.

Table 2 - Fieldbus Interface Pins

Pin Descriptions

Microprocessor/Memory Interface Pins

<u>PIN NAME</u>	<u>PIN #</u>	<u>FUNCTION</u>	<u>REMARKS</u>
PI_AD[19:00]	113-110; 107-100; 98-91	Address bus shared by FB4050, microprocessor and the external memory.	FB4050 fully controls during DMA
PB_DB[15:00]	54-47; 45-38	Data bus shared by FB4050, microprocessor and the external memory.	FB4050 fully controls during DMA
PI_RST	21	An active low signal forces the FB4050 into an initialized state.	
PO_NAD19	114	Logical opposite of PB_AD19	Used to swap upper and lower sections of the flash memory map.
PI_CSFL	115	Chip select for addressing flash memory generated by microprocessor.	Active low.
PO_CSFL	116	Chip select for addressing flash memory through the FB4050.	Active low.
PO_CSFLR	29	Chip select for addressing flash memory through the FB4050.	Active low.
PO_CSRAM	117	Chip select for addressing external memory generated by the FB4050.	Active low, Used only during DMA.
PI_CSFB	119	Chip select for addressing the internal registers of the FB4050.	Active low.
PB_BHE	121	Byte High Enable signal that tells which byte of the 16 bit data bus is to be written into the register.	When in DMA mode, this signal is controlled by the FB4050. Otherwise it controlled by the microprocessor.
PB_WR	120	The write control signal	When in DMA mode, this signal is controlled by the FB4050. Otherwise it is controlled by the microprocessor.

Table 3a - Microprocessor/Memory Interface Pins

Pin Descriptions

Microprocessor/Memory Interface Pins (continued)

PIN NAME	PIN #	FUNCTION	REMARKS
PB_RD	122	The read control signal.	When in DMA mode, this signal is controlled by the FB4050. Otherwise it is controlled by the microprocessor.
PO_HOLD	126	This signal sends a DMA Request to the microprocessor.	Active low.
PI_HLDA	124	The DMA acknowledge from an external device.	Active low; when active, FB4050 has control of address, data and RD and WR lines.
PO_HLDA	125	The DMA acknowledge signal from the FB4050	Active low; can be sent to PI_HLDA of another FB4050 to create a "daisy-chain".
PI_INTR	19	The signal receives an interrupt from an external device.	Active low.
PO_INTR	20	This signal transmits an interrupt to the microprocessor.	Active level low; must be manually reset to remove interrupt and exit int service routine.
PI_BYTE	28	Selects the width of the external data bus; This signal is set by the microprocessor or external circuitry.	Active low.
PI_BOOT	27	Enables boot strap loads	When this signal and PI_RST are both low, the boot loader will bypass the microprocessor chip select signal and load from a pre-determined location.
PI_FLSEL	22	Toggles output of flash memory chip select between PO_CSFL and PO_CSFLR	When "0" selects PO_CSFL When "1" selects PO_CSFLR

Table 3b - Microprocessor/Memory Interface Pins (continued)

Pin Descriptions

LCD Interface Pins

<u>PIN NAME</u>	<u>PIN #</u>	<u>FUNCTION</u>	<u>REMARKS</u>
PO_SEG[47:00]	86-75; 3; 140-129; 68-57; 14-4	LCD segments	160 segments are divided over 4 backplanes onto the 48 segment pins.
PO_BPL0.[2:0]	15,16,17	LCD Backplane 0 pins	Used in different combinations depending on LCD position and time.
PO_BPL1.[2:0]	69,70,71	LCD Backplane 1 pins	Used in different combinations depending on LCD position and time.
PO_BPL2.[2:0]	87,88,89	LCD Backplane 2 pins	Used in different combinations depending on LCD position and time.
PO_BPL3.[2:0]	141,142,143	LCD Backplane 3 pins.	Used in different combinations depending on LCD position and time.
PI_PIN1.[3:0]	74,56,2,128	LCD Pin 1 position	Each PI_PIN1 pin is valid for one distinct LCD position.

Table 4 - LCD Interface Pins

Pin Descriptions

Sensor Interface Pins

<u>PIN NAME</u>	<u>PIN #</u>	<u>FUNCTION</u>	<u>REMARKS</u>
PO_CHCL	23	Output Pin	General purpose output; Can be used to toggle PI_CHIGH or PI_CLOW for input
PI_CLOW	24	Input frequency pulse counter from pulse trap	Can be used to monitor low capacitance reader
PI_CHIGH	25	Input frequency pulse counter from pulse trap	Can be used to monitor high capacitance reader

Table 5 - Sensor Interface Pins

Power Interface Pins

<u>PIN NAME</u>	<u>PIN #</u>	<u>FUNCTION</u>	<u>REMARKS</u>
VCC	37, 109	4050 Power	3.3V
VLC	1, 73	LCD Display Power	Device dependant, typically 3.3V - 5V
GND	18,36,46,55,72,90,99,108,118,127,144	Ground	

Table 6 - Power Interface Pins

Pin Descriptions

Pin Summary

<u>PIN#</u>	<u>NAME</u>	<u>TYPE</u>	<u>PIN#</u>	<u>NAME</u>	<u>TYPE</u>
1	VLC	Power	26	PO_C125	Output
2	PI_PIN1.1	Input	27	PI_BOOT	Input
3	PO_SEG35	Output	28	PI_BYTE	Input
4	PO_SEG00	Output	29	PO_CSFLR	Output
5	PO_SEG01	Output	30	PO_SYNC	Output
6	PO_SEG02	Output	31	PI_PHPDU	Input
7	PO_SEG03	Output	32	PO_RDRF	Output
8	PO_SEG04	Output	33	PO_TDRE	Output
9	PO_SEG05	Output	34	PO_TXEN	Output
10	PO_SEG06	Output	35	PO_PHPDU	Output
11	PO_SEG07	Output	36	GND	Power
12	PO_SEG08	Output	37	VCC	Power
13	PO_SEG09	Output	38	PB_DB00	Bi-Directional
14	PO_SEG10	Output	39	PB_DB01	Bi-Directional
15	PO_BPL0.2	Output	40	PB_DB02	Bi-Directional
16	PO_BPL0.1	Output	41	PB_DB03	Bi-Directional
17	PO_BPL0.0	Output	42	PB_DB04	Bi-Directional
18	GND	Power	43	PB_DB05	Bi-Directional
19	PI_INTR	Input	44	PB_DB06	Bi-Directional
20	PO_INTR	Output	45	PB_DB07	Bi-Directional
21	PI_RST	Input	46	GND	Power
22	PI_FLSEL	Input	47	PB_DB08	Bi-Directional
23	PO_CHCL	Output	48	PB_DB09	Bi-Directional
24	PI_CLOW	Input	49	PB_DB10	Bi-Directional
25	PI_CHIGH	Input	50	PB_DB11	Bi-Directional

Table 7a - Pin Summary

Pin Descriptions

Pin Summary

PIN#	NAME	TYPE	PIN#	NAME	TYPE
51	PB_DB11	Bi-Directional	76	PO_SEG37	Output
52	PB_DB13	Bi-Directional	77	PO_SEG38	Output
53	PB_DB14	Bi-Directional	78	PO_SEG39	Output
54	PB_DB15	Bi-Directional	79	PO_SEG40	Output
55	GND	Power	80	PO_SEG41	Output
56	PI_PIN1.2	Input	81	PO_SEG42	Output
57	PO_SEG11	Output	82	PO_SEG43	Output
58	PO_SEG12	Output	83	PO_SEG44	Output
59	PO_SEG13	Output	84	PO_SEG45	Output
60	PO_SEG14	Output	85	PO_SEG46	Output
61	PO_SEG15	Output	86	PO_SEG47	Output
62	PO_SEG16	Output	87	PO_BPL2.2	Output
63	PO_SEG17	Output	88	PO_BPL2.1	Output
64	PO_SEG18	Output	89	PO_BPL2.0	Output
65	PO_SEG19	Output	90	GND	Power
66	PO_SEG20	Output	91	PB_AD00	Bi-Directional
67	PO_SEG21	Output	92	PB_AD01	Bi-Directional
68	PO_SEG22	Output	93	PB_AD02	Bi-Directional
69	PO_BPL1.2	Output	94	PB_AD03	Bi-Directional
70	PO_BPL1.1	Output	95	PB_AD04	Bi-Directional
71	PO_BPL1.0	Output	96	PB_AD05	Bi-Directional
72	GND	Power	97	PB_AD06	Bi-Directional
73	VLC	Power	98	PB_AD07	Bi-Directional
74	PI_PIN1.3	Input	99	GND	Power
75	PO_SEG36	Output	100	PB_AD08	Bi-Directional

Table 7b - Pin Summary

Pin Descriptions

Pin Summary

<u>PIN#</u>	<u>NAME</u>	<u>TYPE</u>	<u>PIN#</u>	<u>NAME</u>	<u>TYPE</u>
101	PB_AD09	Bi-Directional	128	PI_PIN1.0	Input
102	PB_AD10	Bi-Directional	129	PO_SEG23	Output
103	PB_AD11	Bi-Directional	130	PO_SEG24	Output
104	PB_AD12	Bi-Directional	131	PO_SEG25	Output
105	PB_AD13	Bi-Directional	132	PO_SEG26	Output
106	PB_AD14	Bi-Directional	133	PO_SEG27	Output
107	PB_AD15	Bi-Directional	134	PO_SEG28	Output
108	GND	Power	135	PO_SEG29	Output
109	VCC	Power	136	PO_SEG30	Output
110	PB_AD16	Bi-Directional	137	PO_SEG31	Output
111	PB_AD17	Bi-Directional	138	PO_SEG32	Output
112	PB_AD18	Bi-Directional	139	PO_SEG33	Output
113	PB_AD19	Bi-Directional	140	PO_SEG34	Output
114	PO_NAD19	Output	141	PO_BPL3.2	Output
115	PI_CSFL	Input	142	PO_BPL3.1	Output
116	PO_CSFL	Output	143	PO_BPL3.0	Output
117	PO_CSRAM	Output	144	GND	Power
118	GND	Power			
119	PI_CSFB	Input			
120	PB_WR	Bi-Directional			
121	PB_BHE	Bi-Directional			
122	PB_RD	Bi-Directional			
123	PI_BCLK	Input			
124	PI_HLDA	Input			
125	PO_HLDA	Output			
126	PO_HOLD	Output			
127	GND	Power			

Table 7c - Pin Summary

Memory Mapping

The FB4050 allows the use of both 8-bit memory and 16-bit memory with an address space of up to 20-bits (1 Meg) for 8-bit memory and 19-bits (512K) for 16-bit memory. The signal PI_BYTE must be set appropriately for proper functionality. Memory mapping is microprocessor dependent and will vary depending on which chip select signals are correspondingly connected to the

FB4050's chip select signals. Please refer to the documentation for your specific microprocessor for more details. When PI_CSFB is active low, the internal registers of the FB4050 will appear every 100h over the entire range mapped to that specific chip select signal (microprocessor dependant).

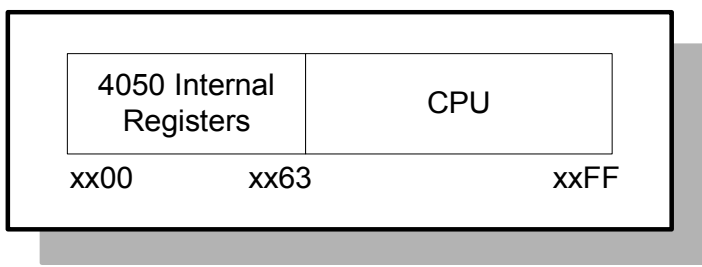


Figure 2 - Typical Memory Map

FB4050 Interface Environment

The figure below represents a typical interface of the FB4050 with a general CPU and external devices. As can be seen, the CPU and FB4050 share a common address and data bus as well as a common clock source. Control signals such as RD, WR and BHE are shared between the FB4050 and the CPU with control delegated to the FB4050 through DMA requests.

When working with frames, it is necessary to use external memory (RAM) in order to perform functions such as storing the received frames, reading the frames to be transmitted and to look for an address match in the address tables.

Both 8-bit and 16-bit memories are supported by the FB4050 and can be selected by PI_BYTE.

Fieldbus messages are received and transmitted through the Medium Attachment Unit (MAU). This unit contains all the analog circuitry needed to interface the FB4050 to the Fieldbus network. Messages are transmitted and received by the FB4050 in Manchester Biphase-L Encoded format. This format, which encodes the clock signal into the data, is decoded into bits upon reception and encoded on transmission automatically by the FB4050.

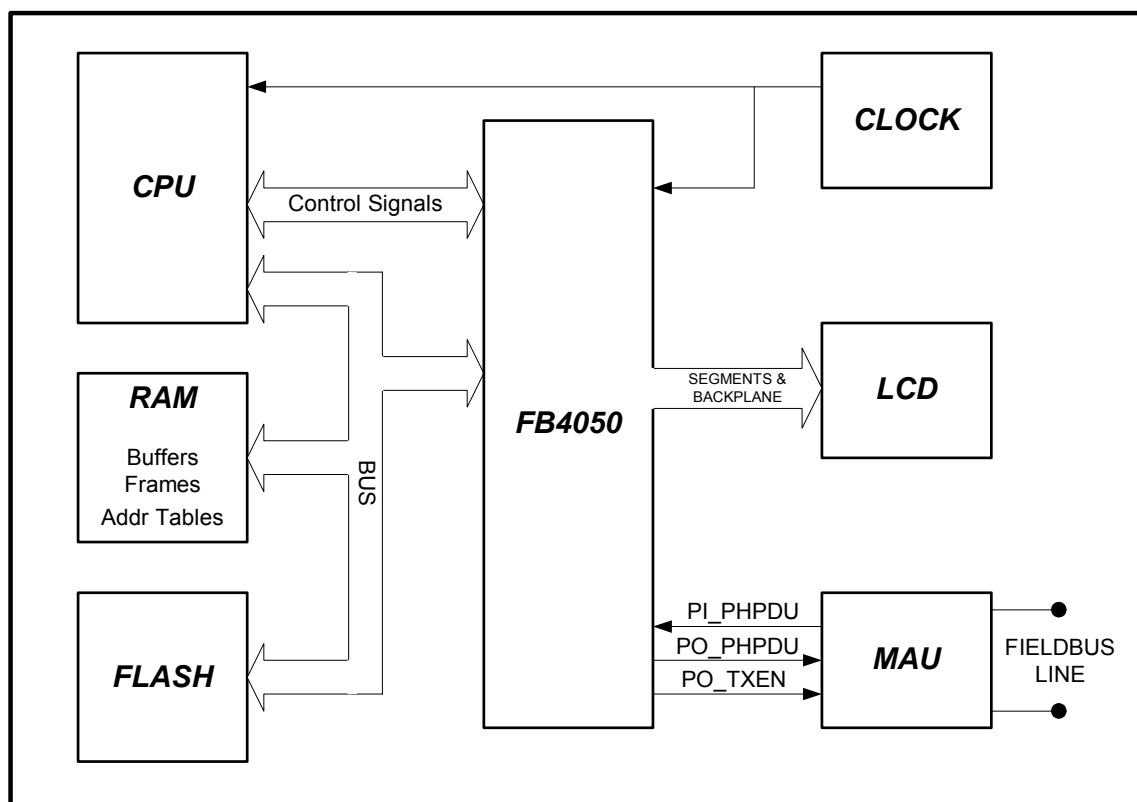


Figure 3 - General CPU Interface

FB4050 CPU Interface

The FB4050 provides a seamlessly interface with the Mitsubishi M16 microprocessor. A boot loader function is also supported. When PI_BOOT and PI_RST are both low, the boot loader will bypass the microprocessor chip select

signal and load from a predetermined location in flash memory.

A typical CPU/FB4050 interface is shown below.

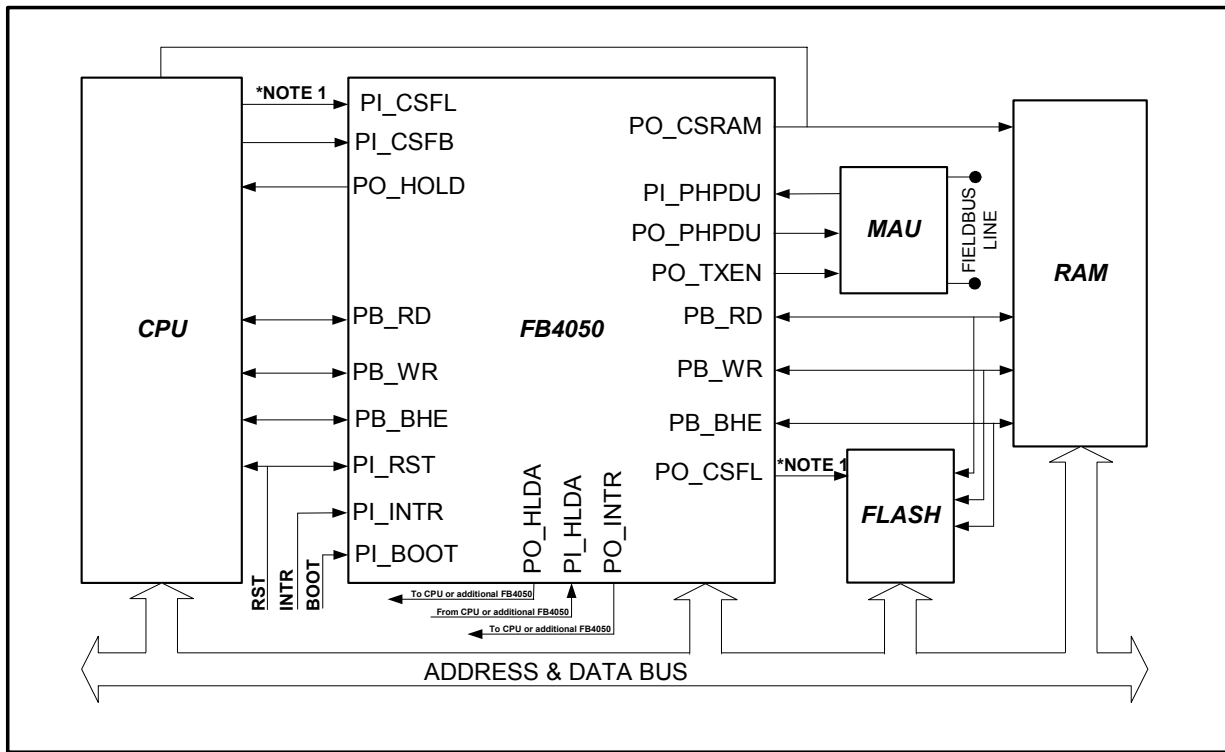


Figure 4 - CPU Interface

***Note 1:** Signals PI_CSFL and PO_CSFL are only required for compatibility with the boot loader. If this functionality is not needed for a particular design, the CSFL signal of the CPU may be connected directly to the flash memory.

Internal Block Diagram

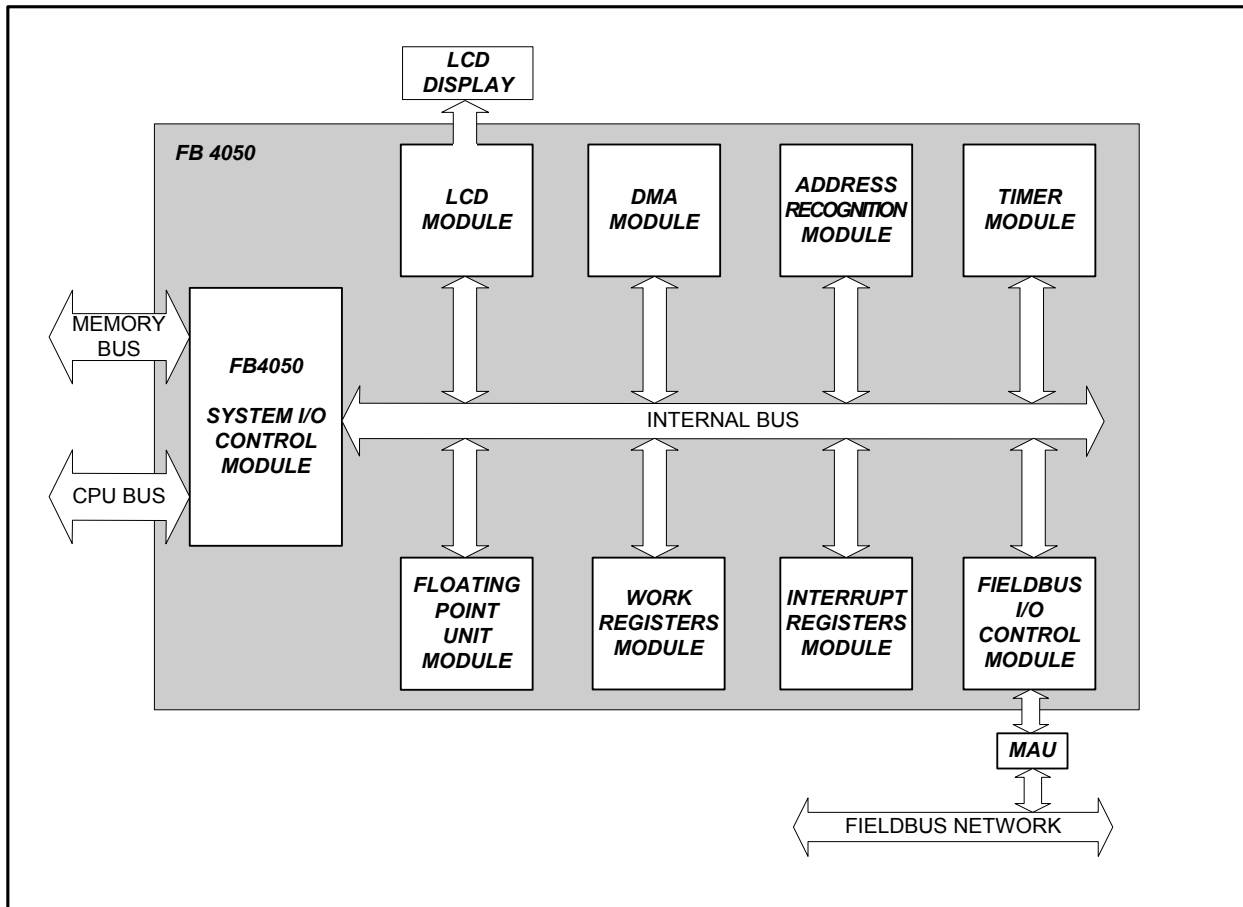


Figure 5 - FB4050 Internal Block Diagram

System I/O Control Module

This module controls the input and output between the FB4050 and the microprocessor. It is responsible for monitoring the input chip select signals and asserting the correct output chip select signals at the appropriate time.

This module is also responsible for enabling the reset conditions of the FB4050 when a PI_RST is asserted and determining what mode the data bus is in (8-bit or 16-bit) from PI_BYTE.

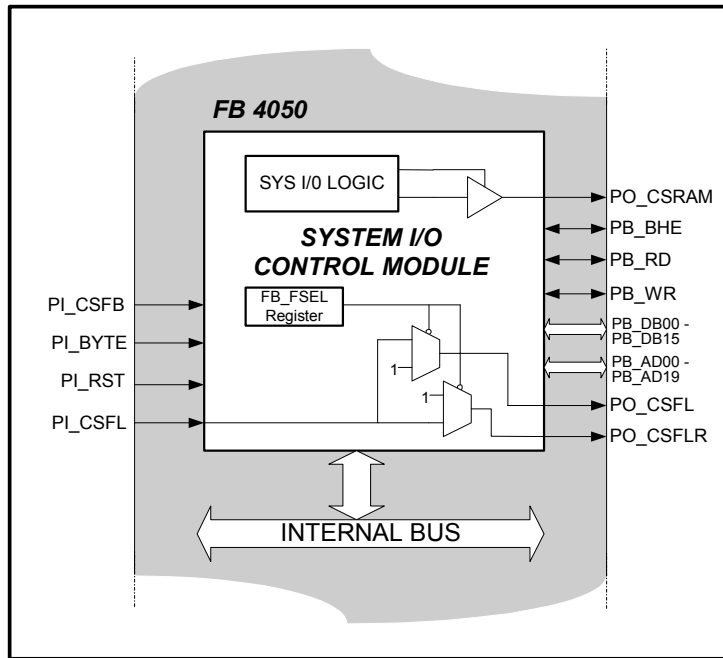


Figure 6 - Fieldbus I/O Control Module

DMA Module

The DMA module controls DMA access. The FB4050 gains access to the address and data busses through a DMA request. A DMA request consists of the FB4050 asserting the PO_HOLD signal active low. The CPU then replies with a DMA acknowledge on PI_HLDA until the DMA access cycle has finished. For the duration of the asserted (active low) DMA acknowledge, the FB4050 has complete control over the address and data bus as well as the control signals RD, WR and BHE. When the FB4050 is finished its DMA cycle, the PO_HOLD signal will return to its inactive state (high), and the CPU will return PI_HLDA

to its inactive state. Every DMA access must be in the PO_CSRAM memory space as set by the CPU memory map. DMA access will not work in any other segments.

When multiple FB4050's are used in the same device the PO_HOLD signals can share the same signal path to the CPU. However, the PO_HLDA signal from the previous FB4050 must be connected to the PI_HLDA of the next FB4050. This effectively forms a "daisy-chain" that will pass along the signal to each controller.

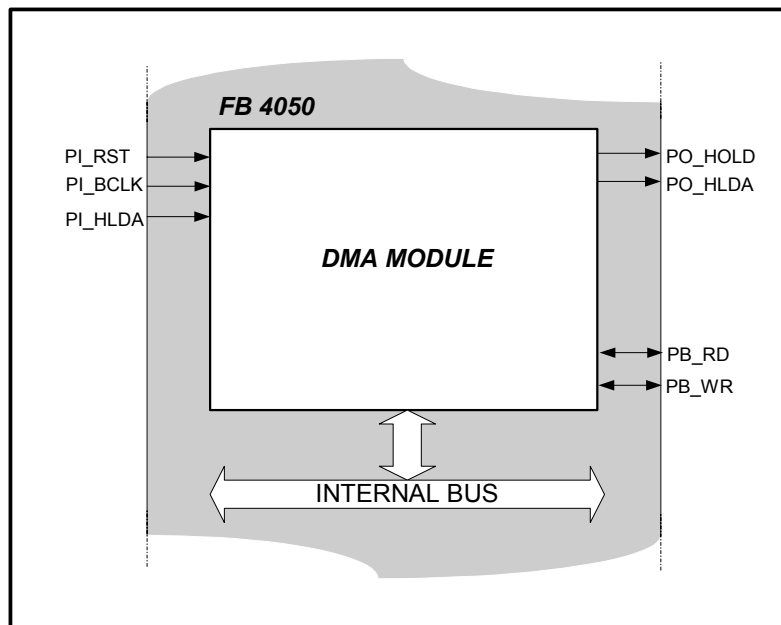


Figure 7 - DMA Module

LCD Module

To minimize the cost associated with the fabrication of displays and still gain the benefits of conventional LCD technologies, an integrated display driver is included in the FB4050. The LCD Module controls the output of the segments and the generation of the 4 backplanes. The module also monitors the orientation of the LCD through the pin1 signals (PI_PIN1.1- PI_PIN1.4). This enables the detection of the display positions (0°, 90°, 180° and 270°) and the reorganization of the data segments on the fly.

The 160 bits of segment information are multiplexed by the FB4050 to the 48 available pins. Note there are an extra 12 pins not used for each orientation of the LCD. However, they are necessary for the

implementation of the free rotate mechanism. Each backplane of the LCD is alternately activated, displaying the segments that are related to it. Displaying any information is just a matter of accessing the right segments distributed over the four backplanes totaling up to 160-bits of display data. Since there are 4 backplanes, each one is sampled at the LCD clock rate divided by 4. The user only needs to set a specific combination of the 160 display data segments to generate a piece of information on the LCD. The generic case of a LCD is having numerical and alphanumeric digits distributed over a thin film of liquid crystal. However, the LCD is a customizable component where each manufacturer can take advantage of their design. (see diagram below)

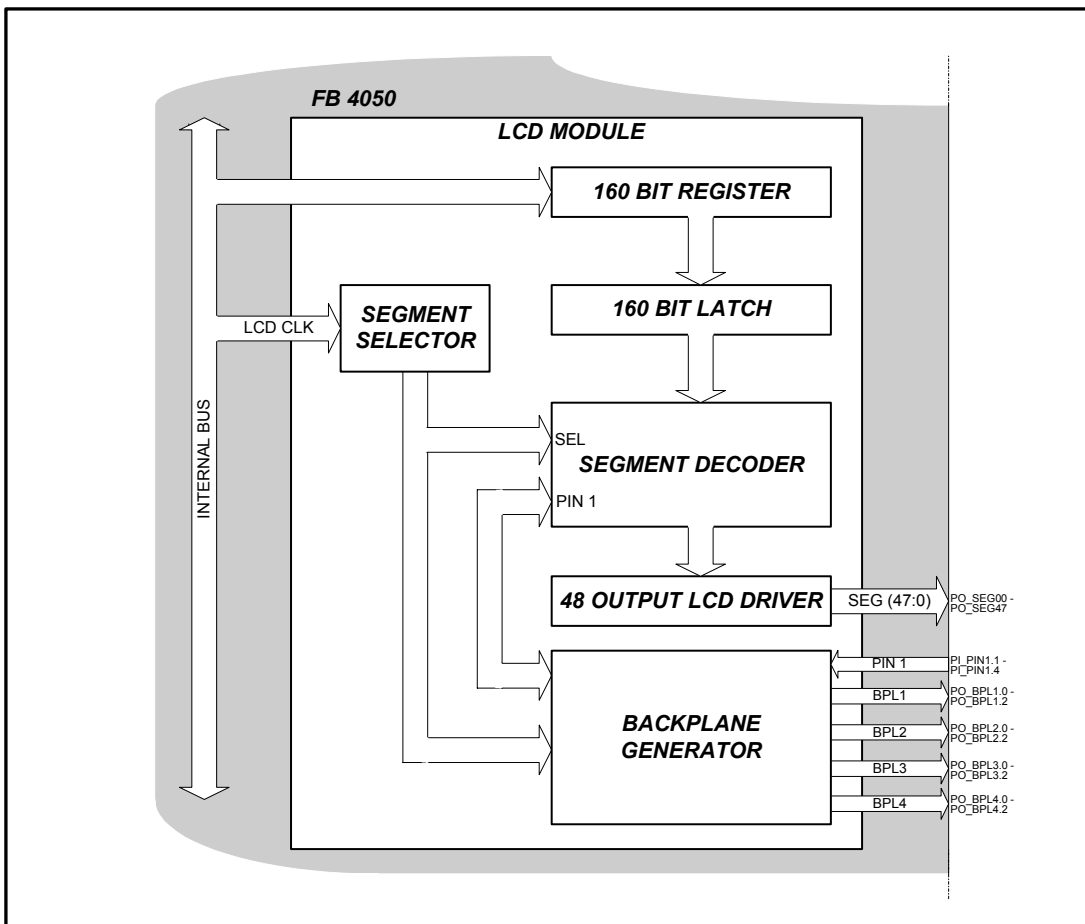


Figure 8 - LCD Module

LCD Module

The following four diagrams detail the correlation of the 160 LCD segments to the 48 FB4050 segment pins for each backplane under every possible 90° rotation. The 48 FB4050 segments pins (PO_SEG_[47:00]) can be seen inside the FB4050 at the center of the diagram along with the backplane pins (PO_BPL0. [2:0] – PO_BPL3.[2:0]) and Pin1 position pins (PI_PIN1[3:0]). The 48 FB4050 segment pins correlate directly to the columns radiating outward from the FB4050. Each column set represents a different rotation of the LCD. The inner set of columns that surround the FB4050

contain the values of the 160 LCD segments that correspond to each of the 48 FB4050 segment pins under a 0° rotation for the corresponding backplane. The columns that radiate outward after the 0° rotation set are for 90°, 180° and 270° rotations respectively. Note that each figure shows only the 40 segments corresponding to one backplane. All 4 figures need to be referenced to determine how all 160 LCD segments are composed and accessed by the available 48 pins. The reference “P” indicates the location of pin 1.

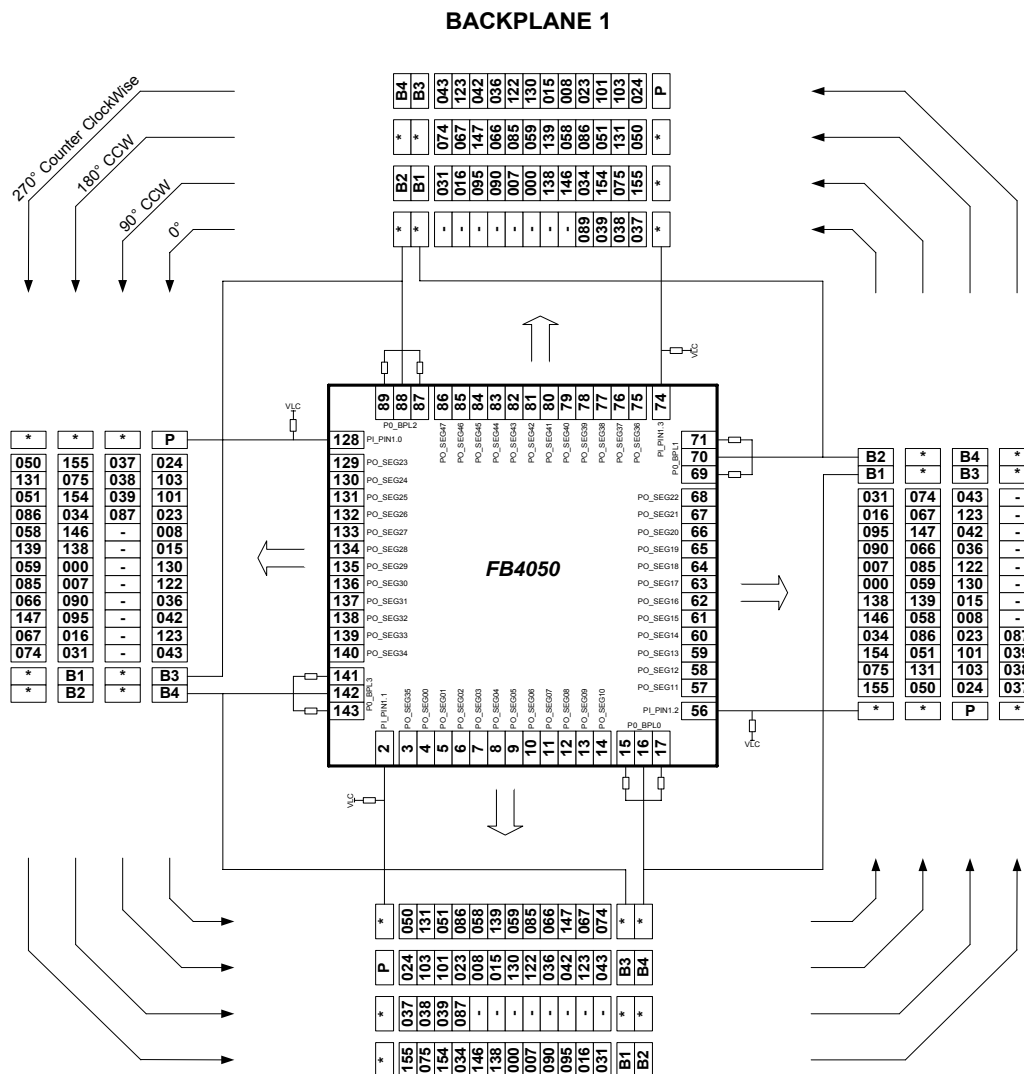


Figure 9 - LCD Backplane 1

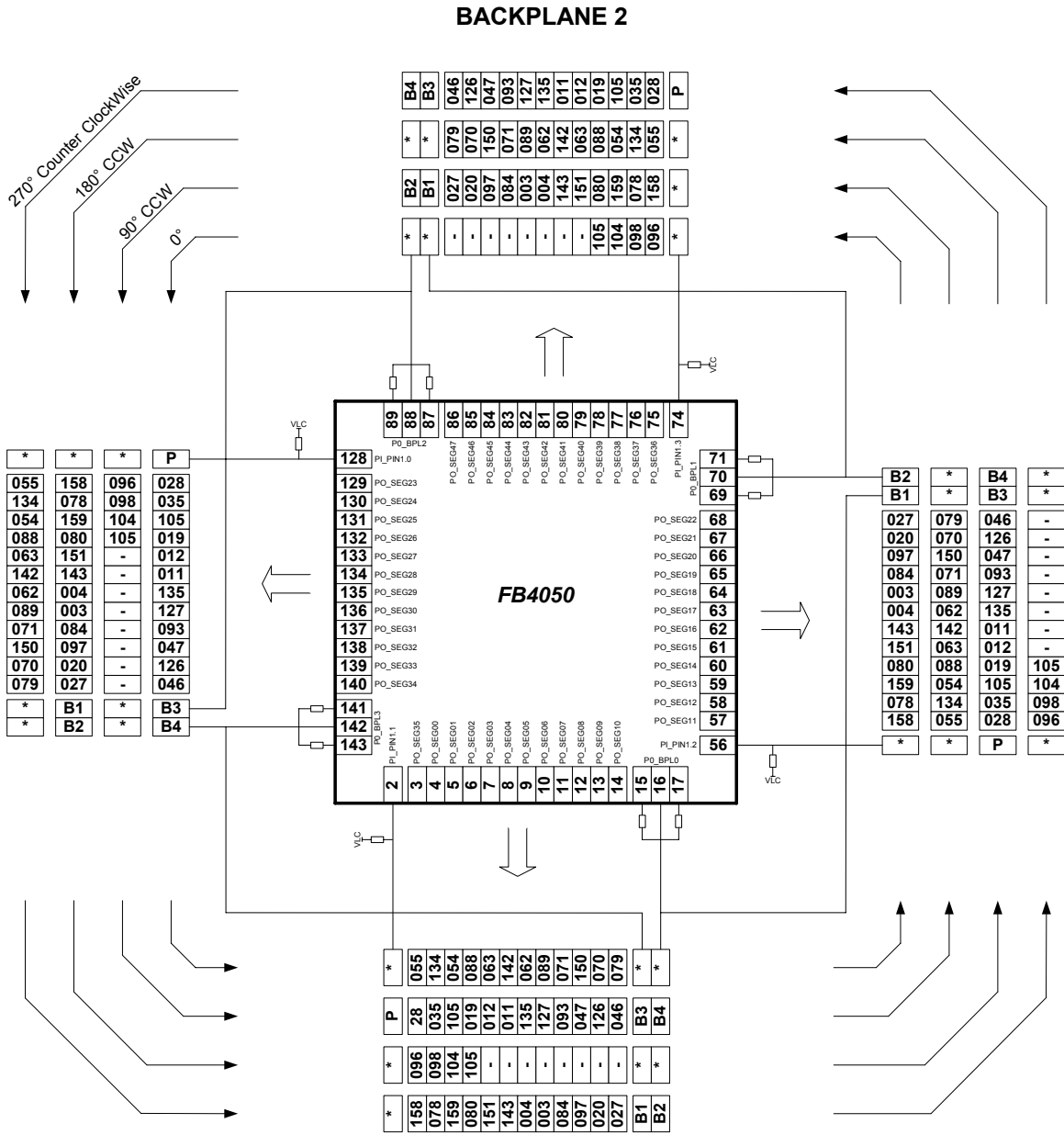
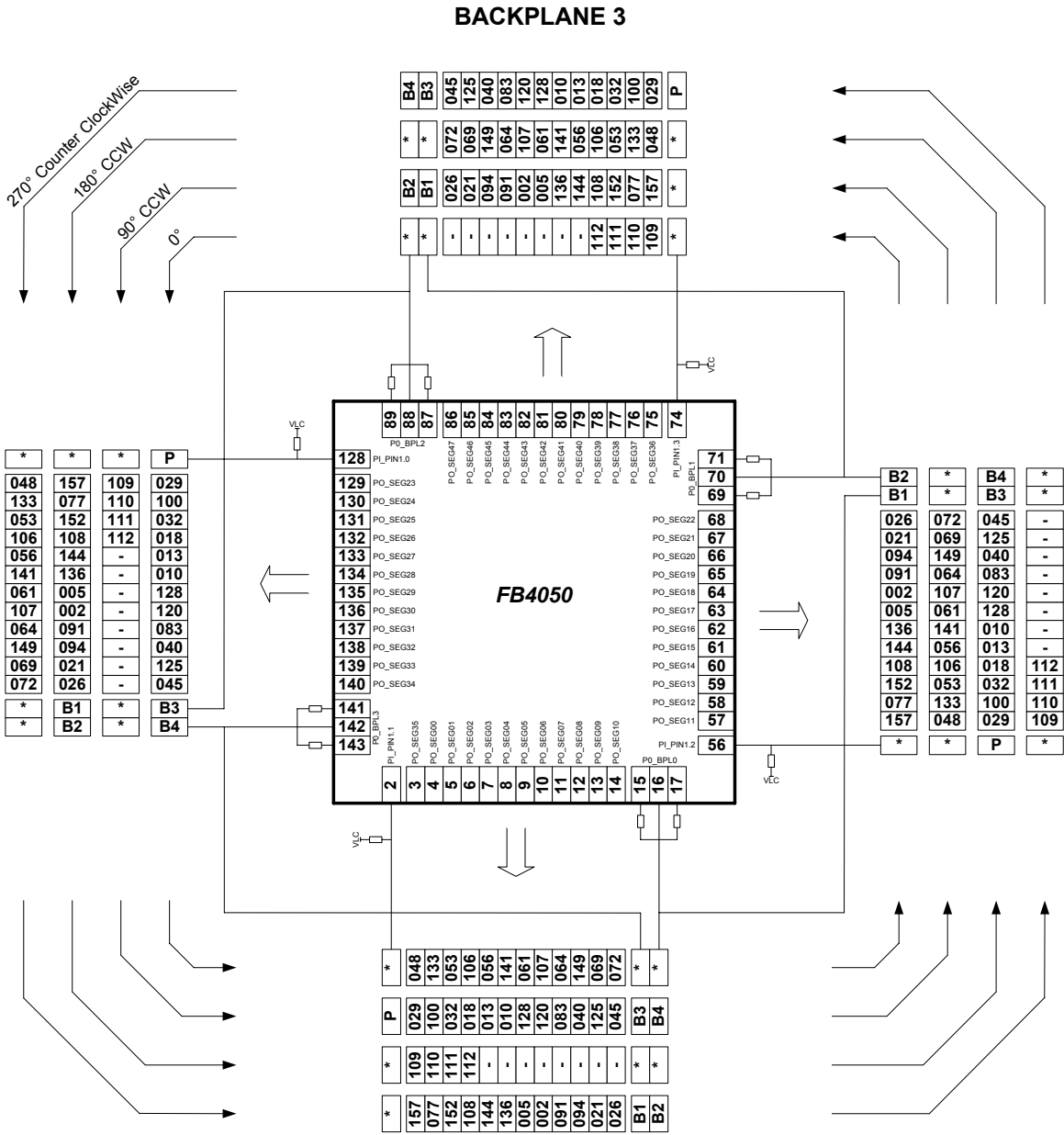


Figure 10 - LCD Backplane 2



BACKPLANE 4

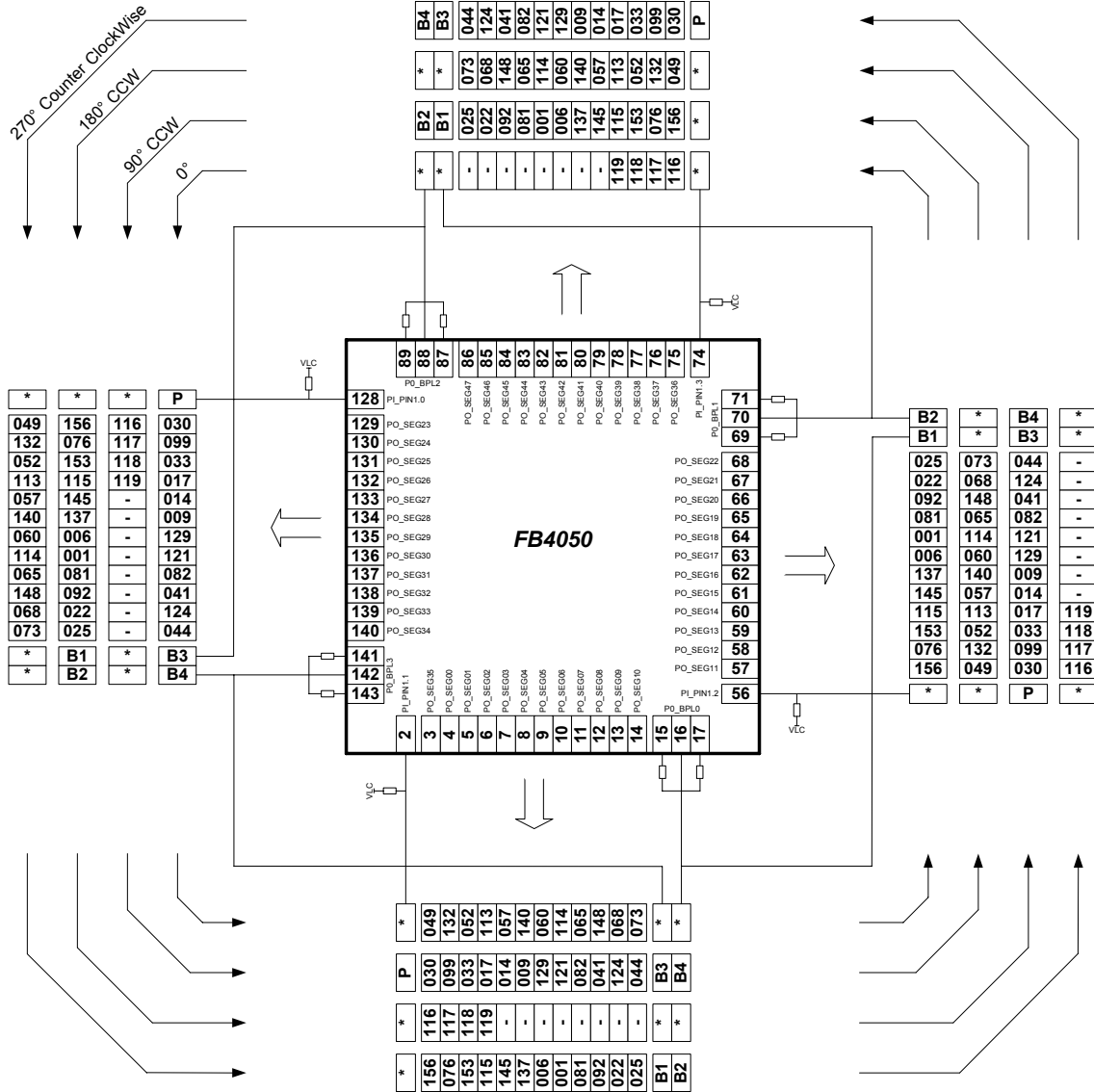


Figure 12 - LCD Backplane 4

Timer Module

The timer module controls the generation of the internal clocks and an external clock of 125 KHz for general purposes. PI_BCLK is the external input clock signal. This signal is then divided by various amounts to create the system clocks: octet, 1/32 ms and 1 ms. PI_RST will clear the timers. The baud rate can

be controlled in software by writing to control register fb_cntrl_2.

The Baud Rate and Clock Generator Module is part of the Timer Module. It selects one of the clock sources and internal clock configurations based on the FB_CNTRL_2 work register.

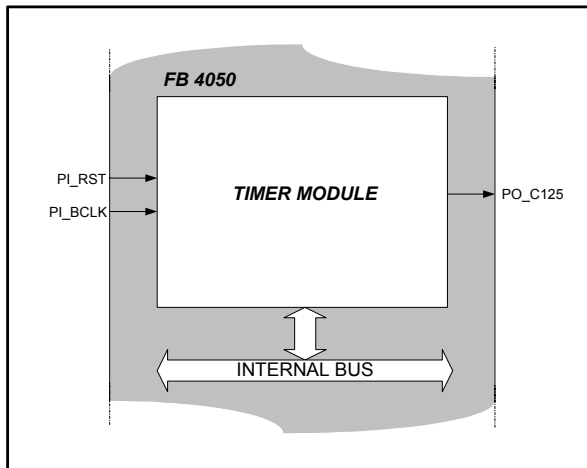


Figure 13 - Timer Module

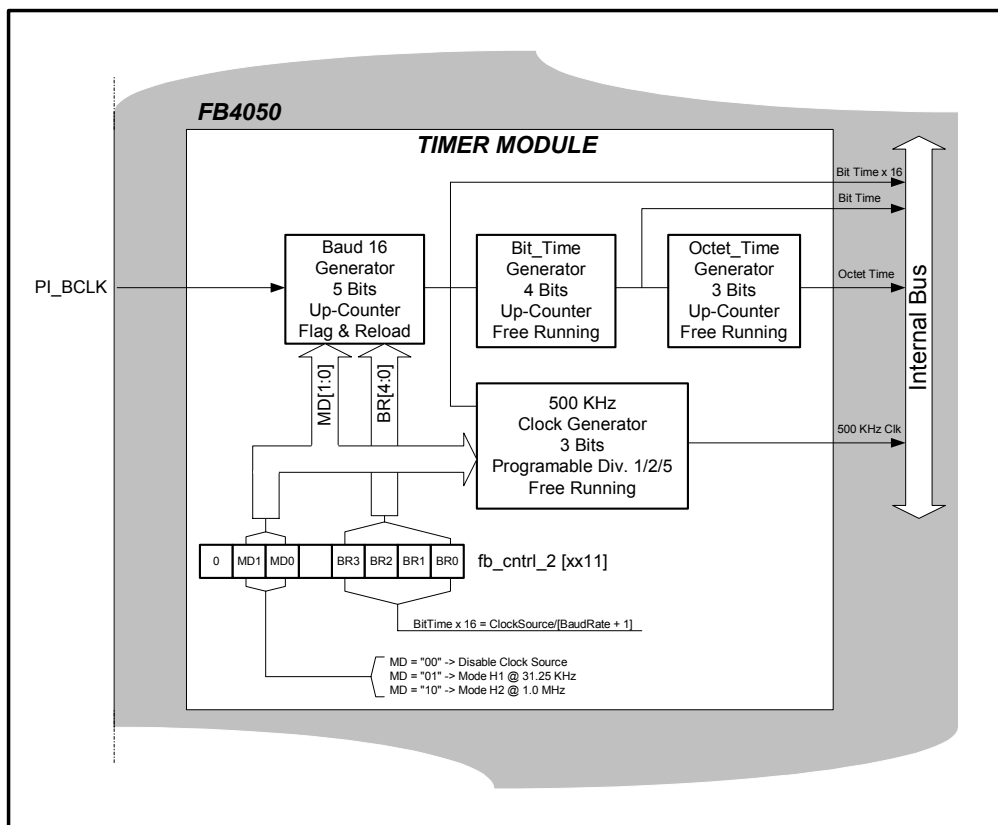


Figure 14 - Baud Rate and Clock Generator Module

Fieldbus Address Recognition Module

The address recognition module is responsible for detecting matches between received messages' Fieldbus Destination Address and tables of addresses in external memory. The Frame Control is extrapolated from the message by this module. The value of the Frame Control determines if the

destination address is compared to an 8-bit value or to tables of 16 or 32-bit values. The address recognition module automatically searches for a match and sets an internal interrupt if one is found. In order to accomplish these tasks, it receives or sends information to or from the I/O Modules.

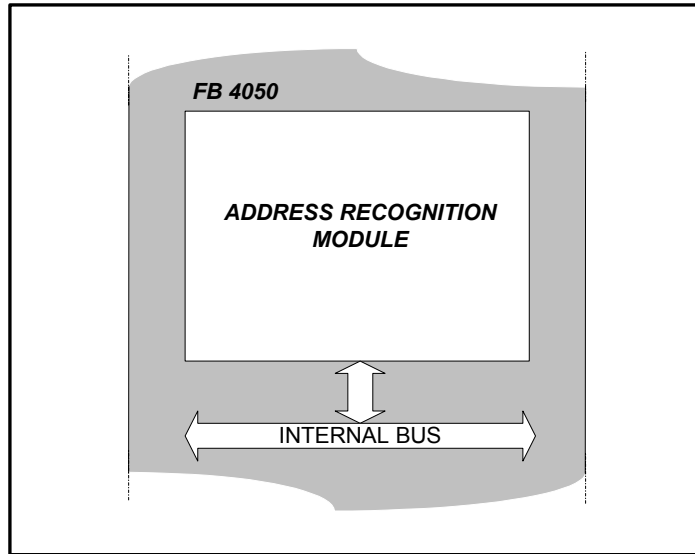


Figure 15 - Fieldbus Address Recognition Module

Fieldbus I/O Control Module

The I/O Control module controls the data flow between the Fieldbus environment and the FB4050. The DMA and System I/O Modules send control signals in order for the module to take the proper action; either receive or transmit information over signals PI_PHPDU and PO_PHPDU respectively. Data that is received or transmitted is Manchester

decoded or encoded respectively. This module also checks the work register fb_cntrl_0 and fb_cntrl_1 to enable features such as DMA transmission/reception or the Interruption Request process. Three status signals are output, PO_TDRE, PO_RDRF and PO_TXEN.

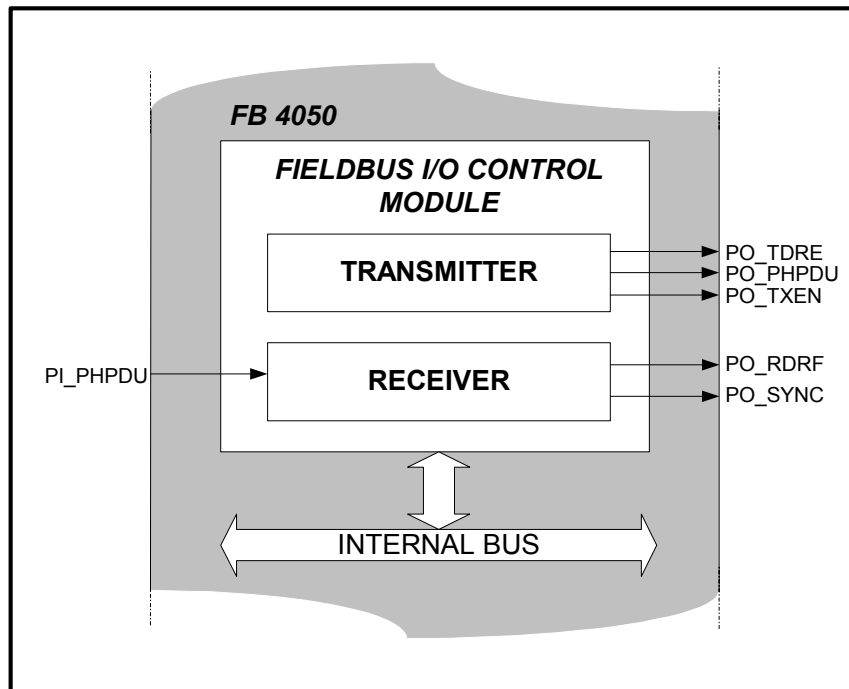


Figure 16 - Fieldbus I/O Control Module

Work Registers Module

This module represents the work registers used by the internal modules (LCD, DMA, Address Recognition, Timers, FPU, Fieldbus I/O, System I/O). Each of these blocks represent special

purpose registers which are comprised of more than one register. These registers are described in greater detail in the *Internal Registers* section.

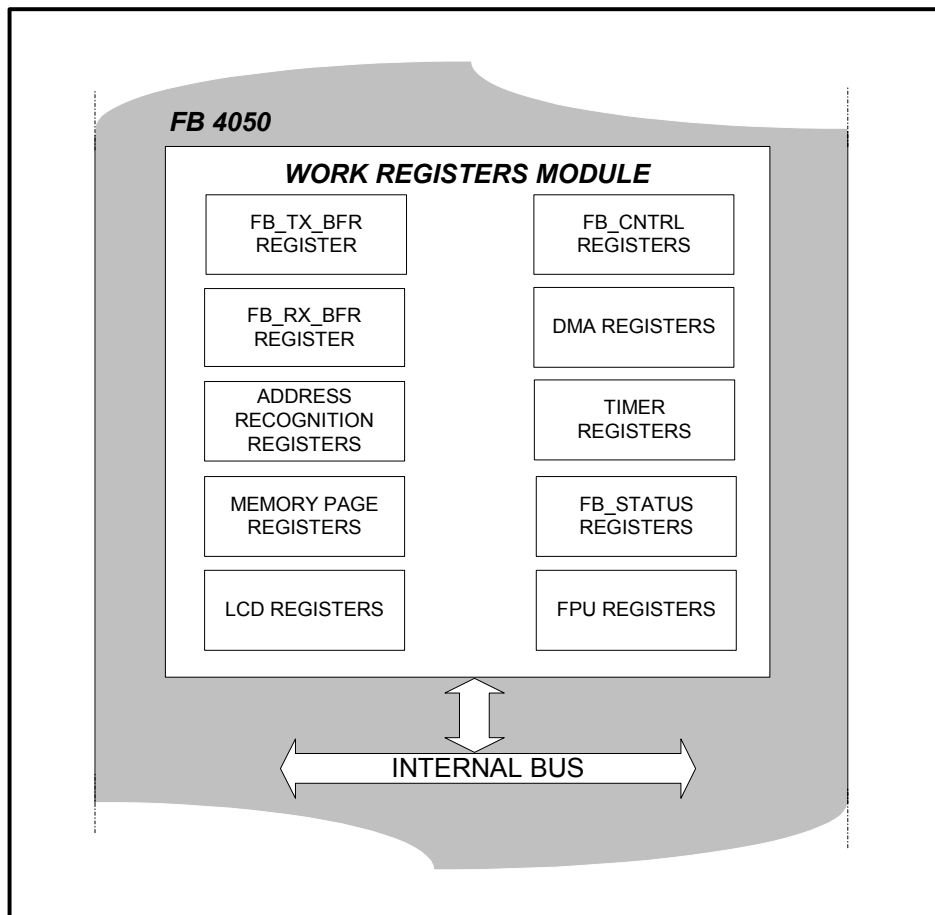


Figure 17- Work Registers Module

Floating Point Unit Module

The floating point unit module is responsible for all floating point calculation in the FB4050. This module cooperates with the system I/O control module to load values into the accumulator registers A and B (fb_flpa_0-fb_flpa_3 and fb_flpb_0-fb_flpb_3). The FPU can perform the operations: addition, subtraction, multiplication, division, integer to float

conversion, float to integer conversion and clear accumulator A. These operations are set in control register fb_flp_cn. The result of the operation is automatically stored over the previous value in accumulator A. In addition, the FPU frequency can be varied by divisions of the input clock by writing to fb_cntrl_3.

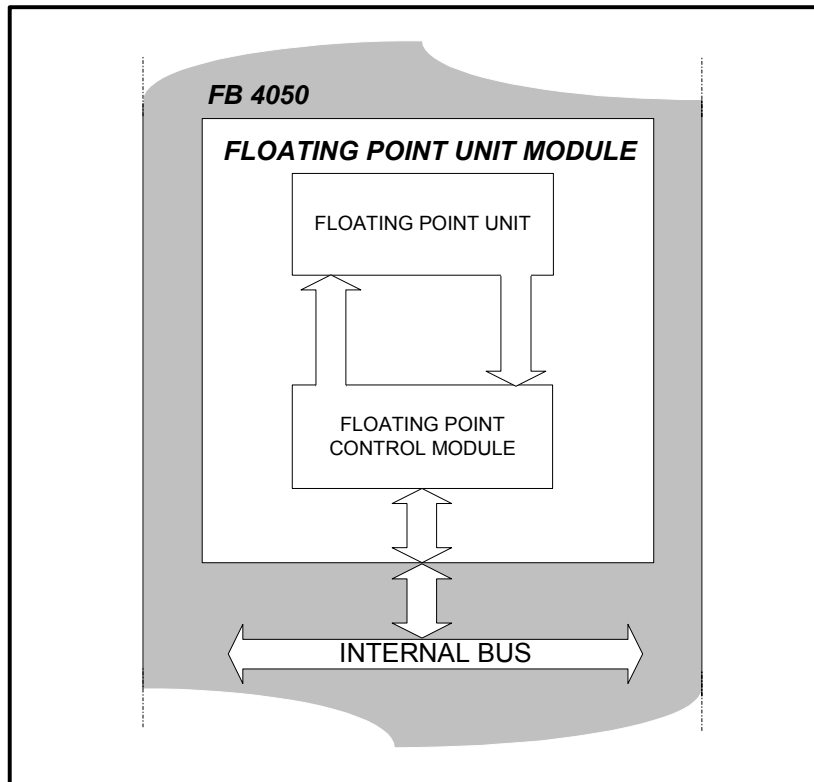


Figure 18 - Floating Point Unit Module

Interrupt Register Module

The interrupt registers module contains all the registers used for flagging interrupts for a given set of conditions. The registers fb_isr_0, fb_isr_1 and fb_isr_2 contain the interrupt flags for the Fieldbus I/O, Address Recognition and Timer Modules respectively. (For information on specific bit assignments for each interrupt register please refer to the *Internal Register Descriptions* section of this document.) When a specific interrupt condition is met, the corresponding flag is set from “0” (the reset state) to “1”. In order to clear an interrupt a “1” must be written to the corresponding bit. This will return the bit to “0” (the reset state). Each individual interrupt can also be masked, effectively “turning off” the interrupt. This is accomplished through the interrupt mask registers, fb_ims_0, fb_ims_1 and

fb_ims_2. Each of these mask registers corresponds to the respective interrupt register (i.e. fb_ims_0 corresponds to fb_isr_0). A specific interrupt can be turned “on” or “off” by writing a “1”(on) or “0”(off) to the corresponding interrupt mask register bit. At reset all interrupts are masked. This module also contains a master interrupt register fb_isr_mst. This register contains one interrupt flag for each interrupt register and also monitors PI_INTR. If an interrupt occurs in any of the interrupt registers or externally from the PI_INTR pin, the master register will set the appropriate flag and signal via PO_INTR an interruption request. Fb_isr_3 and fb_ims_3 are left for future purposes.

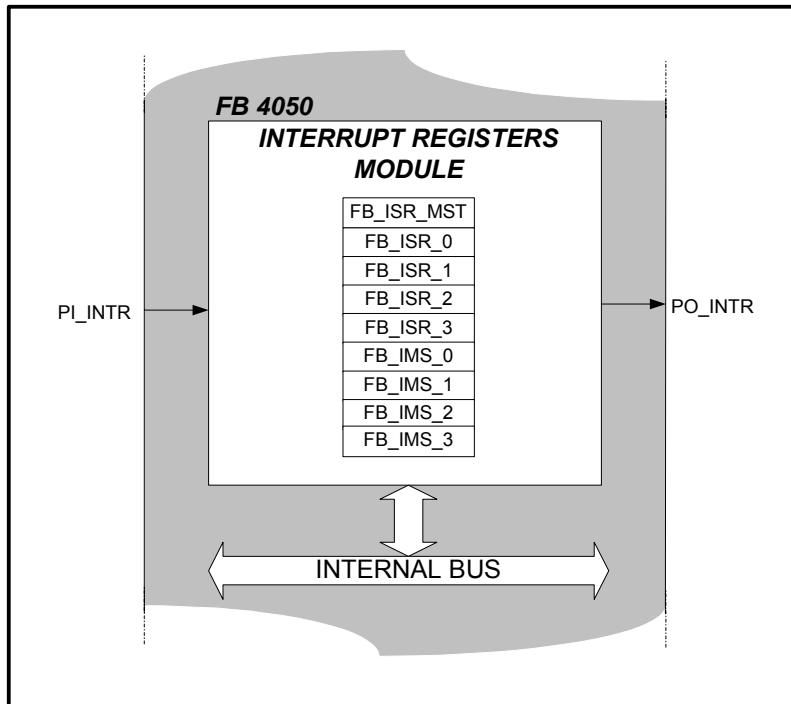


Figure 19 - Interrupt Register Module

Internal Register Operation

When the chip-select is active the FB3050 Controller provides direct access for reading or writing to its internal registers by addressing the desired

register with the least significant six bits of the computer address. The range is XX00H to XX2FH.

<u>ADDRESS</u>	<u>REGISTER NAME</u>	<u>ACCESS MODE</u>	<u>ADDRESS</u>	<u>REGISTER NAME</u>	<u>ACCESS MODE</u>
XX00	FB_RX_BFR	READ	XX18	FB_FRAMECODE	READ
XX00	FB_TX_BFR	WRITE	XX19	FB_TBHL_1	WRITE
XX01	FB_CNTRL_0	R/W	XX19	FB_FRAMECONTROL	READ
XX02	FB_CNTRL_1	R/W	XX1A	FB_TBHL_2	R/W
XX03	FB_ISR_MST	READ	XX1B	FB_NODEID	R/W
XX04	FB_ISR_0	R/W-CLR	XX1C	FB_STATUS_0	READ
XX05	FB_ISR_1	R/W-CLR	XX1D	FB_STATUS_1	READ
XX06	FB_ISR_2	R/W-CLR	XX1E	FB_STATUS_2	READ
XX07	FB_ISR_3	R/W-CLR	XX1F	FB_FSTAT	READ
XX08	FB_IMS_0	R/W	XX20	FB_FRT1 32_0	R/W
XX09	FB_IMS_1	R/W	XX21	FB_FRT1 32_1	R/W
XX0A	FB_IMS_2	R/W	XX22	FB_FRT1MS_0	R/W
XX0B	FB_IMS_3	R/W	XX23	FB_FRT1MS_1	R/W
XX0C	FB_TBCNT_0	R/W	XX24	FB_FRTOCT_0	R/W
XX0D	FB_TBCNT_1	R/W	XX25	FB_FRTOCT_1	R/W
XX0E	FB_TXAD_0	R/W	XX26	NOT USED	NOT USED
XX0F	FB_TXAD_1	R/W	XX27	FB_FLP_CN	R/W
XX10	FB_TXAD_2	R/W	XX28	FB_FLPA_0	R/W
XX11	FB_CNTRL_2	R/W	XX29	FB_FLPA_1	R/W
XX12	FB_RXAD_0	R/W	XX2A	FB_FLPA_2	R/W
XX13	FB_RXAD_1	R/W	XX2B	FB_FLPA_3	R/W
XX14	FB_RXAD_2	R/W	XX2C	FB_FLPB_0	R/W
XX15	FB_CNTRL_3	R/W	XX2D	FB_FLPB_1	R/W
XX16	FB_TBNS_0	WRITE	XX2E	FB_FLPB_2	R/W
XX16	FB_MATCH_0	READ	XX2F	FB_FLPB_3	R/W
XX17	FB_TBNS_1	WRITE	XX30	FB_TCAPL_0	R/W
XX17	FB_MATCH_1	READ	XX31	FB_TCAPL_1	READ
XX1A	FB_TBNS_2	R/W	XX32	FB_TCAPL_2	READ
XX18	FB_TBHL_0	WRITE	XX33	NOT USED	NOT USED

Table 8a - Internal Work Registers

Internal Register Operation (continued)

<u>ADDRESS</u>	<u>REGISTER NAME</u>	<u>ACCESS MODE</u>	<u>ADDRESS</u>	<u>REGISTER NAME</u>	<u>ACCESS MODE</u>
XX34	FB_NPL_0	READ	XX45	FB_LCD_5	WRITE
XX35	FB_NPL_1	READ	XX46	FB_LCD_6	WRITE
XX36	NOT USED	NOT USED	XX47	FB_LCD_7	WRITE
XX37	NOT USED	NOT USED	XX48	FB_LCD_8	WRITE
XX38	FB_TCAPH_0	R/W	XX49	FB_LCD_9	WRITE
XX39	FB_TCAPH_1	READ	XX4A	FB_LCD_10	WRITE
XX3A	FB_TCAPH_2	READ	XX4B	FB_LCD_11	WRITE
XX3B	NOT USED	NOT USED	XX4C	FB_LCD_12	WRITE
XX3C	FB_NPH_0	READ	XX4D	FB_LCD_13	WRITE
XX3D	FB_NPH_1	READ	XX4E	FB_LCD_14	WRITE
XX3E	FB_FLSEL	R/W	XX4F	FB_LCD_15	WRITE
XX3F	FB_CHCL	R/W	XX50	FB_LCD_16	WRITE
XX40	FB_LCD_0	WRITE	XX51	FB_LCD_17	WRITE
XX41	FB_LCD_1	WRITE	XX52	FB_LCD_18	WRITE
XX42	FB_LCD_2	WRITE	XX53	FB_LCD_19	WRITE
XX43	FB_LCD_3	WRITE	XX54	FB_LCD_1D	WRITE
XX44	FB_LCD_4	WRITE			

Table 8b - Internal Work Registers

Internal Registers

Note: Bits with a value of 0 are not used and should be disregarded.

FB_RX_BFR: Receiver Holding Register [xx00]

The Receiver Holding Register stores incoming data from the Fieldbus and presents it to the host microprocessor. When a read at address 00 occurs, the contents of the Receive Holding Register is presented to the data bus for the host microprocessor to read. To avoid receiver overrun or framing errors, the status of the RDRF flag can be monitored either externally on pin PO_RDRF or by reading interrupt status register 0, (fb_isr_0 bit 7). When in DMA mode this process occurs automatically with data written to a pre-assigned area in memory (referenced by fb_rxad_0-fb_rxad_2). This register shares its address with fb_tx_bfr. Thus it can only be read.

FB_TX_BFR: Transmit Holding Register [xx00]

The Transmit Holding Register is written to by the host microprocessor when transmitting to the Fieldbus. When a write at address 00 occurs, data on the data bus is transferred to the internal Transmit Holding Register. To avoid transmitter overrun and insure that the transmitter is ready for a byte of data, the status of the TDRE flag can be monitored either externally on pin PO_TDRE or by reading interrupt status register 0, (fb_isr_0 bit 0). When in DMA mode, this process occurs automatically with data read from a pre-assigned area in memory (referenced by fb_txad_0-fb_txad_2). This register shares its address with fb_rx_bfr. Thus it can only be written.

Control Registers

FB_CNTRL_0 - FB Control Register 0 [xx01]

The FB CONTROL REG 0 is a control register. It has the following command structure and can be read or written.

	7	6	5	4	3	2	1	0
	0	0	RDE	FDM	TDE	TFCE	PSE1	PSE0
RESET	0	0	0	0	0	0	0	0

RDE - Receive Data Enable

Enables the Fieldbus receive data mode.

TFCE - Transmit Frame Check Enable

Enables the transmit frame check mode.

FDM - Full/Half Duplex Mode

Enables the full duplex data mode when high and half duplex mode when low.

PSE1-PSE0 - Preambles Sequence Enable

Enables preamble states (see table 7).

TDE - Transmit Data Enable

Enables the Fieldbus transmit data mode.

<u>PSE1</u>	<u>PSE0</u>	<u>PREAMBLE</u>
0	0	1 Byte Preamble
0	1	2 Byte Preamble
1	0	3 Byte Preamble
1	1	4 Byte Preamble

Table 9 - Preamble Logic

FB_CNTRL_1 - Fieldbus Control Register 1 [xx02]

The FB CONTROL REG 1 is a command register that can be read or written to. It has the following command structure:

	7	6	5	4	3	2	1	0
	0	0	0	WAIT1	WAIT0	DTE	DRE	ARME
RESET	0	0	0	0	0	0	0	0

DTE -DMA Transmit Enable

Used to enable the transmit DMA.

DRE - DMA Receive Enable

Used to enable the receive DMA.

ARME - Address Recognition Mode Enable

Used to enable the address recognition mode. DRE and RDE should be set when this bit is set or the address recognition will not function.

FB_CNTRL_2 - Fieldbus Control Register 2 [xx11]

The CONTROL REG 2 is a command register that can only be written to. It has the following command structure:

	7	6	5	4	3	2	1	0
	0	MD1	MD0	0	BR3	BR2	BR1	BR0
RESET	0	0	0	0	0	0	0	0

MD1-MD0 - Clock Mode Selects

Define the clock mode.

MD1	MD0	Function
0	0	Disable clock source
0	1	Mode H1 @ 31.25 Kbps.
1	0	Mode H2 @ 1.0 Mbps.

Table 10 - Count Mode Logic

BR[3-0] - Baud Rate Selects

These bits represent a divider function. The desired transmission frequency (usually 31.25Kbps) is calculated from the following equation: $BitTime \times 16 = ClockSource / [BaudRate + 1]$. Where BitTime is the transmission frequency, ClockSource is the clock source frequency and the BaudRate (bits 3-0 of fb_cntrl_2) is the divide factor minus 1. For example, with a clock source of 2MHz, a value of "0011" is used for 31.25 Kbit operation. The divide factor will always be BR+1. Setting the baud rate to "0000" will disable the transmission signal.

FB_CNTRL_3: FPU/LCD Control Register 3 [xx15]

This register is a control register that has the following command structure and can be read or written.

	7	6	5	4	3	2	1	0
	0	0	FLPCLK1	FLPCLK0	0	0	LCDCLK1	LCDCLK0
RESET	0	0	0	0	0	0	0	0

FLPCLK[1:0] - Floating Point Unit Clock Rate Selects

These bits select the FPU clock rate for the FPU using the equation: $\text{ClockSource} / \text{PrescaleDivisor} = \text{FPU Clock Rate}$. Where ClockSource is the input clock frequency, PrescaleDivisor is the FLPCLK[1:0] factor and FPU Clock Rate is the FPU operating frequency. The maximum operating frequency of the FPU is 3.68 MHz.

FLP CLK1	FLP CLK0	Prescale Divisor	Example: FPU Clock Rate (KHz) with Input Clock @ 2 Mhz
0	0	4	500
0	1	2	1,000
1	0	1	2,000
1	1	8	250

Table 11 - FPU Clock Rates

LCDCLK[1:0] – LCD Clock Rate Selects

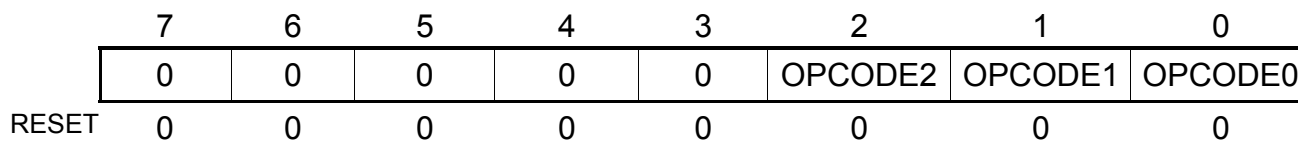
These bits select the LCD clock rate for the LCD driver clock unit using the equation: $\text{ClockSource} / \text{PrescaleDivisor} = 4 * \text{LCD Frequency}$. Where ClockSource is the frequency of the input clock source, LCD Frequency is the desired LCD output display frequency and PrescaleDivisor is bits 1-0 of fb_cntrl_3. The data is actually displayed as the CLK output divided by four due to the 4 backplane signals.

LCD CLK1	LCD CLK0	Prescale Divisor	Example: LCD Clock Rate (Hz) with Input Clock @ 2 MHz
0	0	8192	61.035
0	1	4096	122.07
1	0	2048	244.14
1	1	16384	30.517

Table 12 - LCD Clock Rates

FB_FLP_CN: FPU/LCD Control Register [xx27]

This register is a control register that has the following command structure. Bits 7-4 are read only. Bits 2-0 can be read and written. Bit 3 is not used.



OPCODE[3:0] – FPU Operation Code Selects

The 8 FPU operations and opcodes are below. Once an opcode is written into the register the operation is executed.

OPCODE[2:0]	OPERATION	DESCRIPTION
000	NOP	Null Operation
001	SUB	Subtraction
010	ADD	Addition
011	MUL	Multiplication
100	DIV	Division
101	FLT2INT	Floating Point to Integer Conversion
110	INT2FLT	Integer to Floating Point Conversion
111	CLRA	Clear the contents of Accumulator A

Table 13 - Opcode Descriptions

FB_ISR_MST – Interrupt Status Master Register [xx03]

When read, this register indicates the source of the interrupt.

	7	6	5	4	3	2	1	0
	EIF	0	0	0	0	TISF	AISF	CISF
RESET	0	0	0	0	0	0	0	0

EIF - External Interrupt Flag

Indicates an external interrupt.

TISF - Timer Interrupt Source Flag

When active high indicates that the source of the interrupt is one of the six timer interrupts.

AISF - Address Interrupt Source Flag

When active high indicates that the source of the interrupt is one of the four address lookup interrupts.

CISF - Communication Interrupt Source Flag

When active high indicates that the source of the interrupt is from one of the eight communication interrupts.

FB_ISR_0: Interrupt Status Register 0 [xx04]

This register is a latched value of the communication status signals that have occurred within the FB4050. Writing a logic “1” to any bit in this register will clear its associated contents and remove the interrupt.

	7	6	5	4	3	2	1	0
	RDRF	RAF	RSDF	RDEF	REDF	RIF	TIF	TDRE
RESET	0	0	0	0	0	0	0	0

RDRF - Receive Data Register Full

Active when a data byte has been accumulated.

RAF - Receive Activity Flag

Active high when Fieldbus data is detected.

RSDF - Receive Start Delimiter Flag

Active high when the Start of Header is detected.

RDEF - Receive Data Error Flag

Active high when a receive byte overflow occurs.

REDF - Receiver End Delimiter Flag

Active high when an End of Header is detected.

RIF - Receiver Idle Flag

Active high when a receive message ends.

TIF - Transmit Idle Flag

Active high at the end of a transmission.

TDRE - Transmit Data Register Empty

Active high when the transmitter requests a data byte.

FB_ISR_1: Interrupt Status Register 1 [xx05]

This register is a latched value of the ADDRESS COMPARE status signals that have occurred within the FB4050. Writing a logic “1” to any bit in this register will clear its associated contents and remove the interrupt.

	7	6	5	4	3	2	1	0
	0	0	0	0	RFCF	EOTF	AMDF	B MDF
RESET	0	0	0	0	0	0	0	0

RFCF - Receive Frame Control Flag

Active high when the Frame Control code is detected.

AMDF - Address Match Detection Flag

Active high when an address match is detected.

EOTF - End Of Table Flag

This bit is active high when the end of the address match field is detected. (Table searched without a match)

B MDF - Broadcast Message Detection Flag

Active high when a Broadcast message is detected. (MODE 0)

FB_ISR_2: Interrupt Status Register 2 [xx06]

This register is a latched value of the TIMER status signals that have occurred within the FB4050. Writing a logic “1” to any bit in this register will clear its associated contents and remove the interrupt.

	7	6	5	4	3	2	1	0
	0	0	OCF	OOF	ICF	IOF	1/32CF	1/32OF
RESET	0	0	0	0	0	0	0	0

OCF - Octet Counter Flag

Active high when an Octet count comparison is detected.

IOF - 1 ms Overflow Flag

Active high when the 1 ms count wraps around to a zero value.

OOF - Octet Overflow Flag

Active high when the Octet count wraps around to a zero value.

1/32CF - 1/32 ms Counter Flag

Active high when the 1/32 ms count comparison is detected.

ICF - 1 ms Counter Flag

Active high when the 1 ms count comparison is detected.

1/32OF - 1/32 ms Overflow Flag

Active high when the 1/32 ms count wraps around to a zero value.

INTERRUPT STATUS REGISTER 3

RESERVED

Interrupt Masks

FB_IMS_0, FB_IMS_1, FB_IMS_2: Interrupt Mask Registers [xx08-xx0A]

The Interrupt Mask Registers can be written to or read. A logic one enables the corresponding interrupt while a logic 0 disables the interrupt. When an interrupt source occurs and is enabled, an interrupt generates to the host microprocessor by the PO_INTR pin. The bit definitions are the same as the Interrupt Status register with the corresponding number value.

FB_ISR_3, FB_IMS_3: Interrupt Status/Mask Register 3 [xx07, xx0B]

These registers are for future expansion and are not assigned to any condition.

DMA Related Registers

For more information on DMA procedures, refer to the *FB4050 User Application Notes*.

FB_TBCNT_[1:0]: Transmit Data Count Registers [xx0D,xx0C]

These registers contain the high byte (fb_tbcnt_1) and low byte (fb_tbcnt_0) of the transmit data count. The value loaded is the amount of bytes to be transmitted. The maximum count value is 511, thus only bit 0 of fb_tbcnt_1 can be written. These registers must be loaded to complete a DMA transmission.

FB_TXAD_[2:0]: Transmit Buffer Address Registers [xx10,xx0F,xx0E]

These registers contain the Transmit Buffer data address (MSB-LSB respectively). This value is the address of the location where the bytes to be transmitted are in memory. These registers must be loaded to successfully complete a DMA transmission.

FB_RXAD_[2:0]: Receive Buffer Address Registers [xx14,xx13,xx12]

These registers contain the Receive Buffer data address (MSB-LSB respectively). This value is the address of the location where the incoming bytes are to be received in memory. This location is required to be in the address space of PO_CS RAM. The 3 least significant nibbles of fb_rxad are not writable and thus the receive buffer address must be chosen at the beginning of a 4K block of memory. These registers must be loaded to successfully complete a DMA reception.

Address Recognition Registers

For more information on Address Recognition procedures, refer to the *FB4050 User Application Notes*.

FB_TBNS_[2:0]: NS Table Address Registers [xx1A, xx17, xx16]

These registers contain the address recognition NS table data address (MSB-LSB respectively). This value is the address of the location where the NS table comparisons begin. Fb_tbins_2 and fb_tbhl_2 share the same register, and thus the HL and NS tables must be in the same 64K segment. These registers must be loaded to successfully recognize NS addresses in incoming messages and can only be written.

FB_TBHL_[2:0]: HL Table Address Registers [xx1A,xx19,xx18]

These registers contain the address recognition HL table data address (MSB-LSB respectively). This value is the address of the location where the HL table comparisons begin. Fb_tbins_2 and fb_tbhl_2 share the same register, and thus the HL and NS tables must be in the same 64K segment. These registers must be loaded to successfully recognize HL addresses in incoming messages and can only be written.

FB_MATCH_[1:0]: Match Vector Registers [xx17,xx16]

These registers contain the match vector address high byte (fb_match_1) and low byte (fb_match_0). This value is the address in the address recognition tables where a match was found. These values are only valid if an address match is detected and fb_status_1 indicates either an NS or HL address has been detected. These registers share addresses with fb_tbins_1 and fb_tbins_0 and thus can only be read.

FB_NODEID: NODE ID Registers [xx1B]

This register contains an 8-bit Node ID address. When an incoming message contains an 8-bit address, it is compared to this register. If a match is determined, AMDF will be set in fb_status_1. This register is commonly used to contain the specific device node ID.

FB_FRAMECONTROL: Frame Control Register [xx19]

This register contains the Frame Control byte received in the last incoming message. This register shares an address with fb_tbhl_1 and thus can only be read.

FB_FRAMECODE: Frame Code Register [xx18]

This register contains the Frame Code vector decoded from the last incoming message. This register shares an address with fb_tbhl_0 and thus can only be read. On the next page is a table of values.

Frame Code Descriptions

FCODE	MESSAGE FUNCTION	FCODE	MESSAGE FUNCTION	FCODE	MESSAGE FUNCTION
00000	Establish Connection 1	01011	Exchange Data 2	10110	Probe Node
00001	Establish Connection 2	01100	Data Transfer 1	10111	Probe Response
00010	Disconnect Connection 1	01101	Data Transfer 2	11000	Pass Token
00011	Disconnect Connection 2	01110	Data Transfer 3	11001	Execute Sequence
00100	Reset Connection 1	01111	Data Transfer 4	11010	Return token
00101	Reset Connection 2	10000	Data Transfer 5	11011	Request Interval
00110	Compel Acknowledge 1	10001	Status Response	11100	Claim LAS
00111	Compel Acknowledge 2	10010	Compel Time	11101	Transfer LAS
01000	Compel Data 1	10011	Time Distribution	11110	Wake Up
01001	Compel Data 2	10100	Round-Trip Query	11111	IDLE
01010	Exchange Data 1	10101	Round-Trip Reply		

Table 14 - Frame Code Descriptions

Status Registers

FB STATUS_0: Status Register 0 [xx1C]

This is a read only register that contains the current status of the communication signals.

	7	6	5	4	3	2	1	0
	RDRF	RAF	RSDF	RDEF	REDF	FCSF	TIF	TDRE
RESET	0	0	0	0	0	0	0	0

RDRF - Receive Data Register Full

Active high whenever a data byte has been accumulated.

RAF - Receiver Activity Flag

Active high whenever Fieldbus data is detected.

RSDF - Receiver Start Delimiter Flag

Active high whenever the Start of Header is detected.

RDEF - Receive Data Error Flag

Active high whenever a receive data overflow occurs.

REDF - Receiver End Delimiter Flag

Active high whenever an End of Header is detected.

FCSF - Frame Check Sequence Flag

Active high whenever a receive message ends with a correct Frame Check Sequence.

TIF - Transmit Idle Flag

Active high at the end of a transmission.

TDRE - Transmit Data Register Empty

Active high whenever the transmitter requests a data byte.

FB STATUS_1 - Status Register 1 [xx1D]

This is a read only register that contains the current status of the address compare signals.

	7	6	5	4	3	2	1	0
	HL	NS	RNAF	RPSAF	RFCF	EOTF	AMDF	B MDF
RESET	0	0	0	0	0	0	0	0

HL - 32-Bit Addressing Flag

Active high whenever an HL address is requested.

NS - 16-Bit Addressing Flag

Active high whenever an NS address is requested.

RNAF - Receive Node Address Flag

Active high whenever a message with a Node Address is received.

RPSAF - Receive PSA Flag

This bit is active high whenever a PSA (implicit destination address) message is detected.

RFCF - Receive Frame Control Flag

Active high whenever the Frame Control character is detected.

EOTF - End of Table Flag

This bit is active high when the end of an address table is detected. (Table searched without a match)

AMDF - Address Match Detection Flag

Active high whenever an address match occurs.

B MDF - Broadcast Message Detection Flag

Active high whenever a Broadcast message is detected.

Status Registers

FB_STATUS_2: STATUS REGISTER 2 [XX1E]

This is a read only register that contains the current status of specific signals. These flags are used for debugging purposes only and generally will not be used in the final project.

	7	6	5	4	3	2	1	0
	RSPF	LTAF	0	0	PPOS3	PPOS2	PPOS1	PPOS0
RESET	0	0	0	0	0	0	0	0

RSPF - Reversed Signal Polarity Flag

Active high whenever the polarity of the signal is reversed. It remains valid until the next incoming message.

LTAF - Lockup Table Activity Flag

Active high whenever a look-up request occurs.

PPOS[3:0] – LCD Pin1 Position

These bits store the signals from the PI_PIN[3:0] input pins. The LCD Driver uses these 4 bits to drive the data segments of the LCD accordingly to its position. These are exclusive read only bits so there are only 4 positions available.

PPOS3	PPOS2	PPOS1	PPOS0	LCD Orientation
1	1	0	1	0°
1	0	1	1	90°
0	1	1	1	180°
1	1	1	0	270°

Table 15- LCD Orientation

FB_FSTAT: Floating Point Unit Status Register [xx1F]

This is a read only register that indicates the status of the floating point unit and its results.

	7	6	5	4	3	2	1	0
	FLPRDY	0	0	0	0	INF	NAN	ZER
RESET	0	0	0	0	0	0	0	0

FLPRDY - FPU Ready Flag

This flag indicates if the FPU is currently executing an operation (value of “0”) or if it has completed the operation (value of “1”).

INF – FPU Overflow Flag

This flag indicates an infinite result from the FPU. This flag will be asserted upon an overflow operation or a division by zero operation.

NAN – FPU Not A Number Flag

This flag indicates a not-a-number result from the FPU. This flag will be asserted on an invalid operation according to the IEEE-754 standard.

ZER – FPU Underflow Flag

This flag represents a zero result from the FPU. This flag will be asserted upon an underflow operation.

Timer Registers

For more information on Timer procedures, refer to the *FB4050 User Application Notes*. When reading a timer, it is necessary to first read the low byte followed by the high byte of the timer. This is an inherent feature of the FB4050. When the low byte of a timer is read, the timer subsystem will stop counting and will resume after the high byte is read. In this manner a timer value will not have to be read “on the fly”.

FB_FRT132_[1:0]: 1/32 ms Timer Registers [xx21,xx20]

These registers contain the upper 8-bits (fb_frt132_1) and lower 8-bits (fb_frt132_0) of the 1/32 ms timer counter. Serves as 1/32 ms time comparator when written to.

FB_FRT1MS_[1:0]: 1 ms Timer Registers [xx23,xx22]

These registers contain the upper 8-bits (fb_frt1ms_1) and lower 8-bits (fb_frt1ms_0) of the 1 ms timer counter. Serves as 1 ms time comparator when written to.

FB_FRTOCT_[1:0]: OCTET Timer Registers [xx25,xx24]

These registers contain the upper 8-bits (fb_frtoct_1) and lower 8-bits (fb_frtoct_0) of the octet timer counter. Serves as octet time comparator when written to.

Floating Point Unit Registers

For more information on Floating Point Unit procedures, refer to the *FB4050 User Application Notes*.

FB_FLPA_[3:0]: Accumulator A Registers [xx2B-xx28]

These registers contain the 4 bytes of Accumulator A, the *operand* floating point number, in the order of fb_flpa_0(MSB) – fb_flpa_3(LSB). The FPU stores the results of any mathematical FPU operation in this register set, effectively erasing the previous value in Accumulator A.

FB_FLPB_[3:0]: Accumulator B Registers [xx2F-xx2C]

These registers contain the 4 bytes of Accumulator B, the *operator* floating point number, in the order of fb_flpb_0(MSB) – fb_flpb_3(LSB). The content of this register set is not affected after a mathematical FPU operation.

FB_FLP_CN: FPU/LCD Control Register [xx27]

See the *Control Registers* section of this document.

FB_CNTRL_3: FPU/LCD Control Register 3 [xx15]

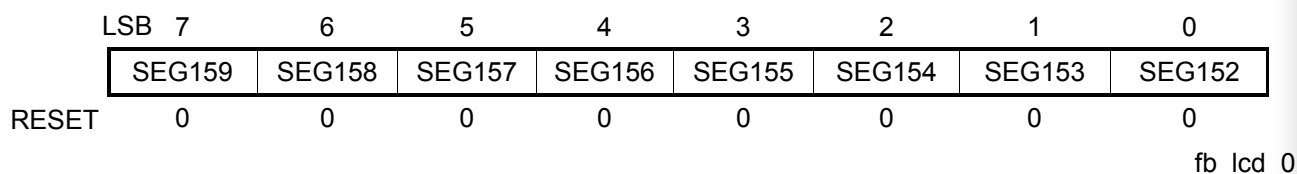
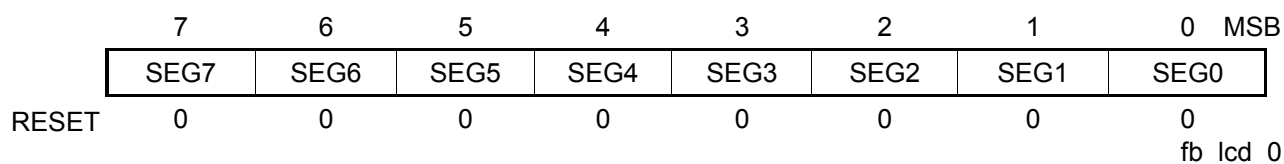
See the *Control Registers* section of this document.

LCD Registers

For more information on LCD procedures, refer to the *FB4050 User Application Notes*.

FB_LCD_[19:0]: LCD Segment Registers [xx53-xx40]

These are a set of 20 8-bit write only registers that comprise the entire 160 segments of the LCD. All 20 registers have the same structure. The diagrams below describe the most and least significant registers. To display information on the LCD, it is necessary to select the segments that will be “on” and the segments that will be “off” with 1’s and 0’s respectively.



FB_LCD_LD: LCD Latch Register [xx54]

This register is the write only register responsible for latching the data to the display. The data that is intended to be displayed must first be loaded into fb_lcd_[19:0] from the MSB to LSB registers. Once this is completed, fb_lcd_ld can be written with a dummy value to act as a trigger for the 160-bit latch to hold all current bit values.

FB_FLP_CN: FPU/LCD Control Register [xx27]

See the *Control Registers* section of this document.

FB_CNTRL_3: FPU/LCD Control Register 3 [xx15]

See the *Control Registers* section of this document.

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